Brandenburgische Technische Universität Cottbus-Senftenberg
Fakultät I
MINT Mathematik, Informatik, Physik, Elektro- und Informationstechnik
Institut für Informatik
Fachgebiet Verteilte Systeme/Betriebssysteme

EINLADUNG zum GASTVORTRAG

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„Recent research topics in the Signals & Systems for Computing (SiSC) Group“

am: Donnerstag, dem 13.06.2019,

ab: 14:30 Uhr

Ort: VG 1C, Seminarraum 0.01

Alle Interessenten sind herzlich eingeladen!

Abstract:

The presentation is split in two parts. First, we address research on the development of a combined ionizing radiation & electromagnetic interference test procedure to achieve reliable integrated circuits. Then, in the second part, we focus research on the development of a new approach to support mixed-criticality workload execution and a fault-free task scheduling algorithm in a multicore processor-based embedded system.

Part I: International standards have been proposed and used to test Integrated Circuits (ICs) for Total-Ionizing Dose (TID) and Single-Event Upset (SEU) as well as for Electromagnetic Interference (EMI). Nevertheless, these standards are separately applied to the IC or electronic system, one after the other, and do not take into account the combined effects of these types of radiation may take over the ICs. In more detail, there is no standard that rules combined tests for TID, SEU and EMI. This topic addresses this lack of product quality information and develop a new methodology to improve the reliability of ICs by performing combined tests for TID, SEU and EMI. We also present recent experimental results from combined measurements we performed on a commercial FPGA IC widely used in critical embedded applications such as aerospace and automotive. Such results strongly suggest that the effects of radiation are not negligible and should be taken into account if one intends to design reliable embedded systems.

Part II: Recently, the use of multicore processors in general-purpose real-time embedded systems has experienced a huge increase. Unfortunately, critical applications are not benefiting from this type of processors as one could expect. The major obstacle is that we may not predict and provide any guarantee on real-time properties of software running on such platforms. The shared memory bus is among the most critical resources, which severely degrades the timing predictability of multicore software due to the bus access contention between cores. This part of the talk presents the current research state on a new approach to support mixed-criticality workload execution in a multicore processor-based embedded system. The approach is based on the use of an infrastructure intellectual property (I-IP) core named Deadline Enforcement Checker (DEC), implemented in hardware, which automatically manages the execution of any number of cores in a TDMA-based bus access police while guaranteeing critical task schedulability. This approach allows the exploitation of the maximum performance offered by a multiprocessing system while guaranteeing critical task schedulability, i.e., that the critical task execution will not violate timing deadline. A case-study based on a quad-core version of the LEON3 softcore processor was implemented in VHDL language. Practical experiments demonstrate the proposed technique is very effective on combining system high performance with critical task schedulability within timing deadline. We also present a second functionality of the DEC I-IP, which aims at monitoring the scheduling process in an Operating System (OS). A preliminary case-study is under implementation, where the OS is running the Early Deadline First (EDF) task scheduling algorithm. The goal of the DEC I-IP, in this case, is to detect faults that escape detection by the native fault detection mechanisms embedded in the OS kernel.