

22.7 A 90% Peak Efficiency Single-Inductor Dual-Output Buck-Boost Converter with Extended-PWM Control

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Power management in portable devices demands small size, low cost as well as long battery lifetime, which in turn drive the development of single-inductor multiple-output (SIMO) converters [1-5]. Due to the battery voltage variation during usage and the wide-range dynamic voltage scaling (DVS) applied for power reduction, high-efficiency buck-boost conversion is required to extend the battery lifetime. The buck-boost converter in [6] selects the operation mode by comparing the output with the supply voltage, which is not suitable for multi-output converters. The reported single-inductor dual-output (SIDO) buck-boost converter in [4] uses a state machine with sophisticated current sense for mode selection and requires a freewheeling state that dissipates energy. The converter in [3] uses one additional auxiliary inductor for step-up/down mode adjustment. This paper proposes an extended-PWM (EPWM) control which automatically selects buck or boost mode and facilitates smooth mode transition. It is suitable for flexible outputs and maintains a high efficiency in buck and in boost converters.

Figure 22.7.1 shows the overall architecture of the SIDO buck-boost converter. It consists of five switches in the power stage: S1, S2, and S3 regulate the total transferred energy by buck/boost conversion; S4 and S5 distribute the energy stored in the inductor to both outputs. All switches are controlled by PWM signals which are generated in two control loops. The converter is specified for two outputs from 1 to 5V with the maximum total power of 2.5W and supply voltage ranging from 2.5 to 5V. The switching frequency is 2MHz. The external inductor is 2.2μH and the capacitor is 20μF each.

Controlling the five power switches in the topology of Fig. 22.7.1 requires three independent duty-ratio signals. A switching converter with PWM control usually generates a duty-ratio signal by comparing the error amplifier output V_{ea1} with a sawtooth waveform $Saw1$. In a buck converter the PWM signal D_{1a} also represents the relation between output and supply voltage, thus $D_{1a} = V_{out}/V_g$. However, this equation is only valid when $V_{ea1} < V_{saw1}$. If $V_{ea1} > V_{saw1}$, the transferred energy is not enough to supply the outputs in buck mode. The converter has to enter into its boost mode, where $D_{1a} = 1$ and D_{1b} is modulated. The proposed EPWM control achieves automatic buck/boost mode selection by considering the relation of V_{ea1} and V_{saw1} . As shown in Fig. 22.7.2, there are two sawtooth waveforms used for D_{1a} and D_{1b} generation. When $V_{ea1} < V_{saw1}$, $Saw2$ is just the same as $Saw1$. When $V_{ea1} > V_{saw1}$, $Saw2$ ramps up to the amplitude of V_{ea1} while $Saw1$ turns to ground. The buck signal D_{1a} is always generated by comparing V_{ea1} with $Saw1$, while the boost signal D_{1b} is only high when V_{ea1} is higher than V_{saw1} . An equivalent PWM signal D_{eq} can be expressed by the two signals: $D_{eq} = D_{1a} + D_{1b} = V_{ea1}/V_{saw1} = V_{out}/V_g$, which extends the conversion ratio concept from a buck to a general switching converter.

Due to parasitic effects of the PWM signal generation, there would be a pulse-skipping problem when D_{eq} is close to 1. A small voltage is added on $Saw1$ as level-shift to overcome this problem. The level-shift leads to an overlap of buck and boost mode, which results in a buck-boost mode for smooth transition. Figure 22.7.2 shows the duty-ratio signal generation of the SIDO buck-boost converter with EPWM control. The buck switches S1 and S2 are controlled by D_{1a} , while the boost switch S3 is controlled by D_{1b} . The output switches S4 and S5 are controlled by D_2 and are only valid when S3 is off. The distribution PWM signal D_2 is generated by comparing V_{ea2} with $Saw1$. As shown in Fig. 22.7.2, the total duration of charging outputs is kept constant (T_c) whether in buck or in boost mode. The mode transition has little influence on the V_{ea2} loop, which helps to attenuate the interaction between the two control loops of the SIDO system. Hence, the proposed EPWM control is also suitable for multiple-output converters.

Figure 22.7.3 shows the schematic of the sawtooth waveform generator of the EPWM control. At the rising edge of the $Pulse$ signal, V_{ea1} and $Saw2$ are compared and the result is used for mode selection. When in buck mode, the sawtooth pull-down signal $dn2$ is the same as $dn1$. In boost mode, $dn2$ is only triggered when $Saw2$ reaches V_{ea1} . As described in Fig. 22.7.2, the EPWM control combines constant-frequency buck mode and constant-off-time boost mode. By adding a phase and frequency detector (PFD) and charge-pump block, a PLL can be built to keep the switching frequency synchronized with an external clock. The bandwidth of the PLL is designed to be lower than that of the SIDO control loop, which provides a pseudo constant-off-time boost mode to make the system compensation easier.

The SIDO converter is a multi-loop feedback system. The power-stage small-signal modeling and system decoupling analysis have been described in [5]. As illustrated in Fig. 22.7.1, a VLX filter is used for the V_{ea1} loop compensation. $VLX1$ and $VLX2$ have a direct response to the PWM signals without the delay of inductor current integration, which makes it suitable for system compensation in switching converters. Low-pass filters are added at both nodes and an active feedback amplifier is used for the differential signal extraction. The VLX-filter-based compensation method in Fig. 22.7.4 is suitable for both buck and boost situations.

The converter is fabricated in a 0.25μm 2P4M CMOS process. The die area is 2.62.9mm². Each output can be used as step down or up conversion. Figure 22.7.5 shows the measured waveforms of output ripples and $VLX1$ and $VLX2$ node voltages in different modes. The output ripple including its spike is lower than 80mV for all situations. $VLX1$ is switched to ground in buck mode, while $VLX2$ is switched to ground in boost mode. In the buck-boost mode, both $VLX1$ and $VLX2$ are switched, which results in more power loss (about 4% efficiency deterioration). The operation mode of the SIDO converter is also determined by the load currents when the converter has one buck and one boost outputs. A load response measurement ($I_L = 42mA \rightarrow 140mA$) in Fig. 22.7.6 shows the transient mode transition between buck and boost mode with load current change. The dynamic measurement also reveals that the EPWM-controlled buck-boost converter may achieve faster response than the conventional buck and boost converters due to the wide modulation range of D_{eq} . The peak power efficiency of 90% is reached at a supply voltage of 3V and when the two outputs are set to 1.8V/214mA and 5V/150mA. By using the proposed EPWM control, the SIDO converter keeps a high efficiency over 80% over a wide output range and includes an automatic mode transition.

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Reference:

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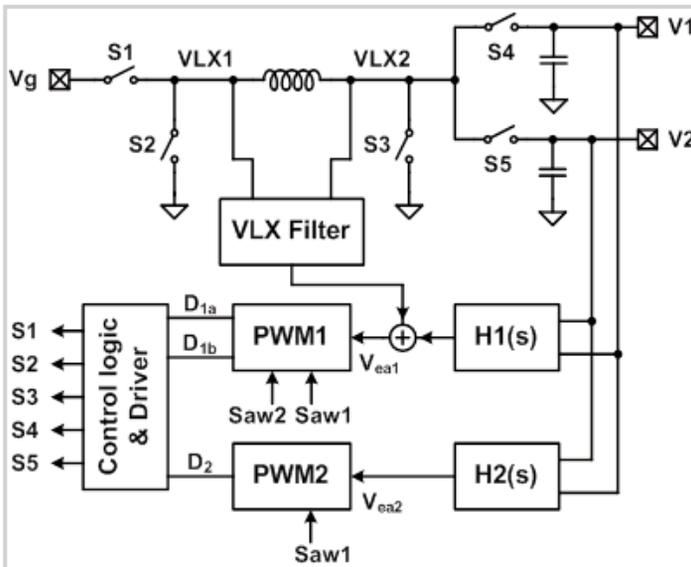


Figure 22.7.1: Architecture of the SIDO buck-boost converter.

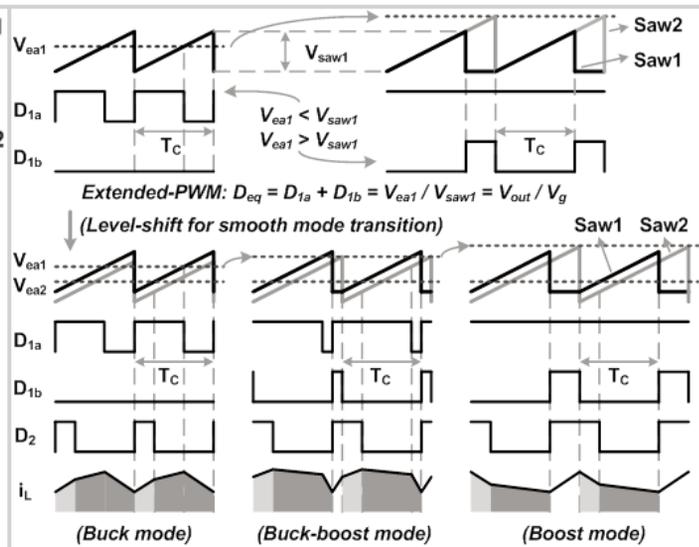


Figure 22.7.2: Scheme of extended-PWM (EPWM) control for buck-boost conversion.

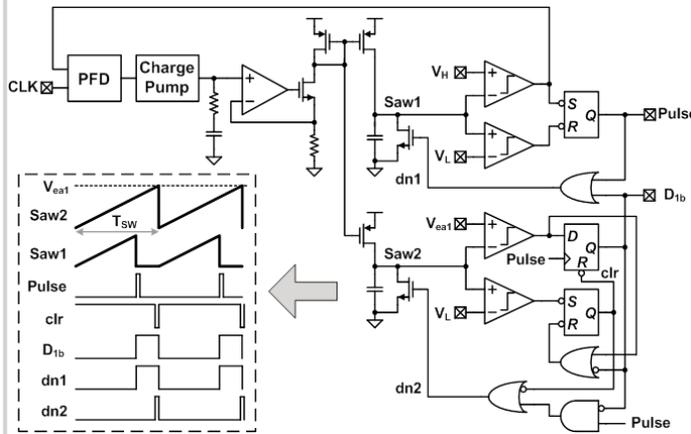


Figure 22.7.3: Schematic of sawtooth waveform generator for EPWM control.

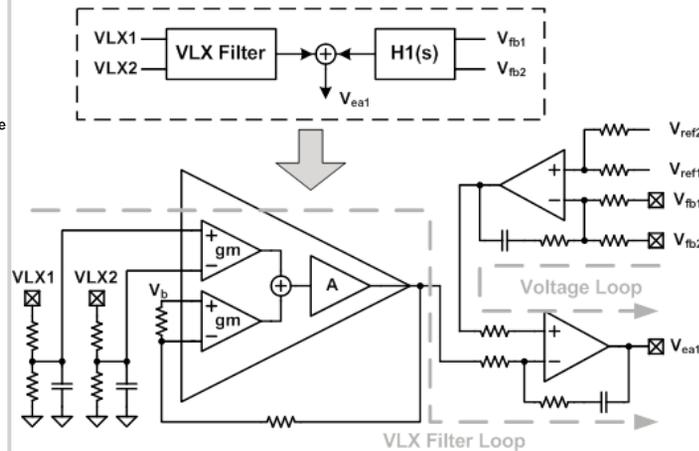


Figure 22.7.4: Schematic of VLX-filter-based compensation.

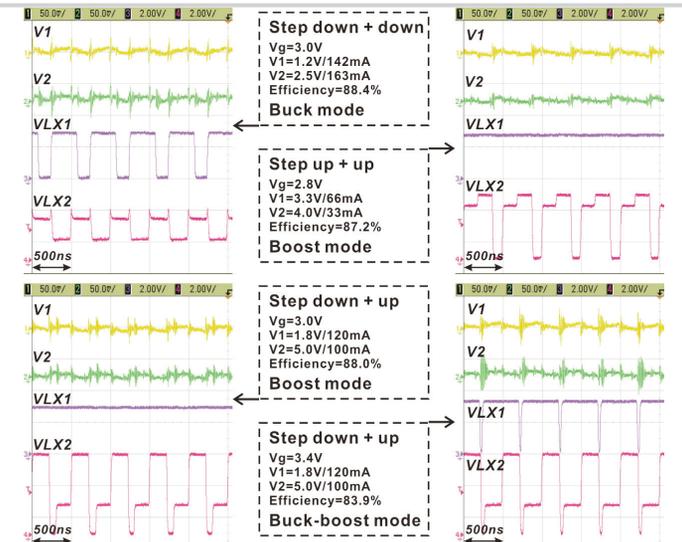


Figure 22.7.5: Measured waveforms of steady-state ripples and node voltages in different modes.

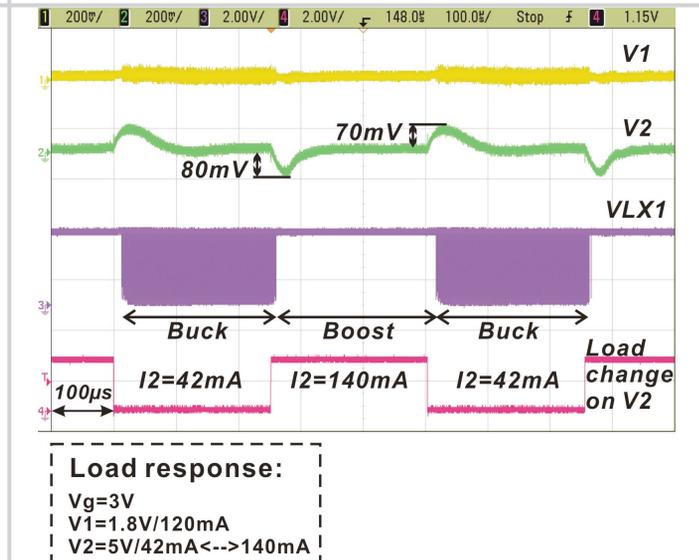


Figure 22.7.6: Measured waveform of dynamic response and mode transition.



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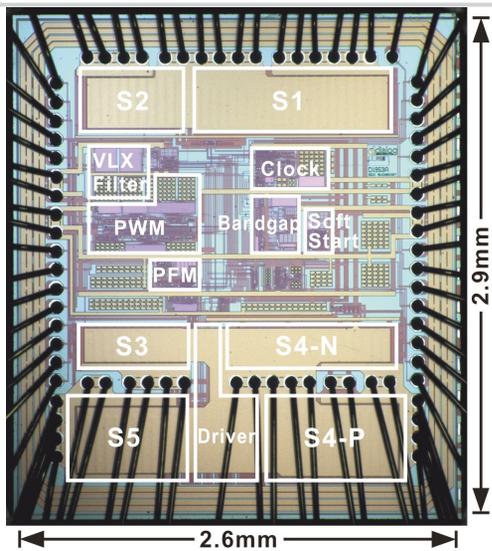


Figure 22.7.7: Micrograph of the SIDO buck-boost chip fabricated on a 0.25 μ m CMOS process.

