A Single-Inductor Dual-Output Switching Converter with Low Ripples and Improved Cross Regulation

Weiwei Xu*, Ye Li*, Xiaohan Gong*, Zhiliang Hong* and Dirk Killat#
*State Key Laboratory of ASIC & Systems, Fudan University, Shanghai, P.R.C.
#Brandenburg University of Technology, Cottbus, Germany

***Abstract*— This paper proposes a novel fly capacitor method for single-inductor dual-output (SIDO) switching converters to reduce the output ripples and spikes. An adaptive common-mode control is presented to suppress the cross regulation problem. The converter can automatically switch between pulse-width modulation (PWM) and pulse-frequency modulation (PFM) control to improve the efficiency. The SIDO converter is specified for one channel 1.2 V/400 mA and the other 1.8 V/200 mA with input voltage ranging from 2.7 V to 5 V. The chip has been fabricated on a 0.25 μm CMOS mixed signal process. The conversion efficiency is 82% at a total output power of 840 mW while the output ripples are about 20 mV and spikes less than 40 mV.**

I. Introduction

Portable applications usually need different supply voltages for different functional modules to minimize power consumption. A more interesting and efficient solution is to use one converter with a single inductor to generate multiple outputs, which reduces the external components and saves cost.

There have been several kinds of single-inductor multiple-output (SIMO) switching converters reported in recent years. The converters in [1] and [2] make use of time-multiplexing control, which suffer from large current ripples and dissipate energy during the freewheeling state. The solution in [3] employs the ordered power-distributive control which has a main channel for compensation and other sub-channels controlled just by comparators. This simplifies the control loop, but has larger ripples and is only suited for small load currents. The converter in [5] works in continuous conduction mode (CCM) and adopts several PWM controllers driven by suitable linear combinations of output errors, which can sustain large load currents, but has large ripples (150 mV) and serious cross regulation (120 mV) problems. So, the existing SIMO converters realize multiple-output with some parasitic effects:

- Load currents are limited by the intrinsic requirement of discontinuous conduction mode (DCM) and pseudo-CCM (PCCM) control.
- Large ripples and spikes, resulting from discontinuous current change on filter capacitors with parasitic series inductors.
- Cross regulation: the SIMO converter can be regarded as a multi-input multi-output system with cross regulation items.
- Efficiency: more switches added in the power path result in more power loss. The efficiency gets worse especially under light loads.

To solve or suppress such problems, a novel adaptive common-mode control and a fly capacitor method are proposed for SIDO switching converters. Section II describes the control strategy and design considerations on ripples and cross regulation problems. System implementation is addressed in section III. The measurement results in section IV will confirm the proposed control methods. A brief conclusion is given in section V.

II. Considerations on SIDO Switching Converters

A. Power Stage and Control Sequence

A conventional buck converter consists of two power switches and one inductor, which provide efficiency power conversion. A dual-output converter is achieved by adding another two switches at the output node of the inductor, which is shown in Fig. 1.

Fig. 2 illustrates the control sequence and the waveforms of the steady-state inductor current and output ripples in CCM. Differing from the comparator-based distributive structure in [3], the controller here employs both PWM generators on control signal D_1 and D_2, which has the advantage of large load currents and comparatively low ripples. However, as pointed out in [1], there will occur serious cross regulation problems.

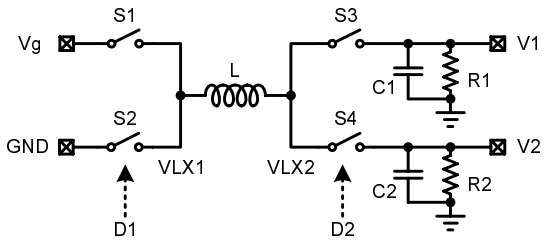

Fig. 1. Power stage structure of SIDO buck converter.

B. Cross Regulation

In a SIMO converter, variation of load current on one channel will affect the others, for all outputs share a single inductor. This is the cross regulation problem, which is one of the severest challenges in SIMO converter design. To solve this problem, the converters in [1] and [2] work in DCM or PCCM with a freewheeling state of inductor current, which makes two channels independent of each other. However, this method is not suitable for the SIDO converter in CCM.

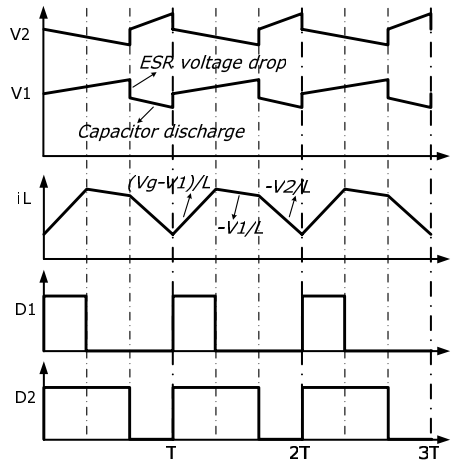

Fig. 2. Waveforms of output ripples and inductor current with control signals.

The converter in [4] regulates the common-mode voltage ($V_{CM} = (V_1 + V_2)/2$) and the differential-mode voltage ($V_{DM} = V_1 - V_2$) instead of two outputs to partly suppress the cross regulation. As shown in Fig. 3, there are two main control loops in the system: the common-mode loop which regulates the total energy by D_1, and the differential-mode loop which distributes the energy in the inductor by D_2. It has been analyzed in [4] that the transfer functions $G_{21}(s)$ and $G_{12}(s)$ represent for the cross regulation items.

Based on the idea of decomposing this cross regulated multi-loop system into several single-loop sub-systems with weak interactions, a novel adaptive common-mode control method is proposed. Here, V_{CM} is adjusted according to the load currents, which can be expressed as:

$$V_{CM} = D_2 V_1 + (1 - D_2) V_2. \tag{1}$$

The weighted coefficient of each channel is proportional to the load current. It is reasonable that the channel which draws more current should have a larger impact on the regulation of inductor current. According to the control sequence in Fig. 2 and assuming the ripples are negligible, the small signal behavior of the SIDO power stage can be described by state

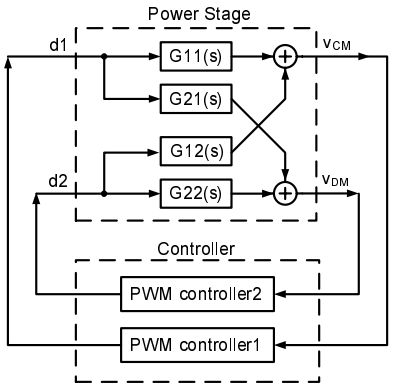

Fig. 3. Small signal structure of SIDO system.

space equations as:

$$\frac{d}{dt}\begin{bmatrix} v_1 \\ v_2 \\ i_L \end{bmatrix} = \begin{bmatrix} -1/R_1C_1 & 0 & D_2/C_1 \\ 0 & -1/R_2C_2 & (1-D_2)/C_2 \\ -D_2/L & -(1-D_2)/L & 0 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \\ i_L \end{bmatrix} + \begin{bmatrix} 0 & I_L/C_1 \\ 0 & -I_L/C_2 \\ V_g/L & (V_2-V_1)/L \end{bmatrix}\begin{bmatrix} d_1 \\ d_2 \end{bmatrix} \tag{2}$$

$$\begin{bmatrix} v_{CM} \\ v_{DM} \end{bmatrix} = \begin{bmatrix} m_1 D_2 & m_2(1-D_2) & 0 \\ m_1 & -m_2 & 0 \end{bmatrix}\begin{bmatrix} v_1 \\ v_2 \\ i_L \end{bmatrix} + \begin{bmatrix} 0 & m_1V_1 - m_2V_2 \\ 0 & 0 \end{bmatrix}\begin{bmatrix} d_1 \\ d_2 \end{bmatrix}$$

where m_1 and m_2 are the feedback coefficients. The transfer functions of power stage can be solved from Eq. 2. The bode plot comparison of $G_{12}(s)$ in Fig. 4 shows that the proposed adaptive common-mode control has about 20dB improvement on the suppression of cross regulation in low frequency (when $V_g = 4\ V, R_1 = 3\ \Omega, R_2 = 90\ \Omega$).

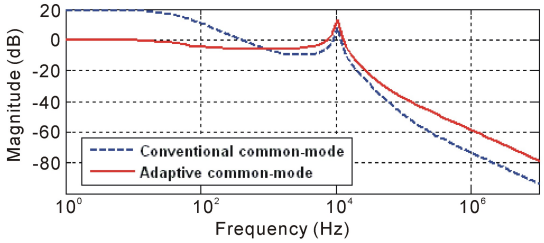

Fig. 4. Bode diagram comparison of $G_{12}(s)$.

C. Ripples

A SIDO buck converter has larger output ripples than a conventional buck converter especially under heavy loads, for the current ripples of filter capacitors in SIDO converters are the total load currents. As shown in Fig. 2, the output ripples mainly consist of two parts: the charge of filter capacitors and the voltage drop on the equivalent series resistor (ESR) of capacitor. When the inductor current switches to one channel, the filter capacitor is charged while the other is discharged. So, the ripples of two outputs are always in inverse phase.

Another serious problem is large spikes, which are caused by the rapid current change on the equivalent series inductors (ESLs) of filter capacitors when switching S3 and S4. They are even larger than output ripples in SIDO converters (e.g. about 100 mV in [6]). As shown in Fig. 5, when the inductor current switches between two outputs, there occur large undershot and overshot spikes on filter capacitors.

Based on the conclusion that the ripples and spikes of two outputs are inverse-phased, a fly capacitor across two outputs can be added to reduce the steady state ripples. The proposed SIDO structure with a fly capacitor is depicted in Fig. 5. The value of the fly capacitor needs careful selected, since it provides an AC path between two outputs, which would deteriorate the performance of cross regulation. Analysis and

simulation shows $C_f = 0.1C_1$ is a good trade-off between ripples and cross regulation.

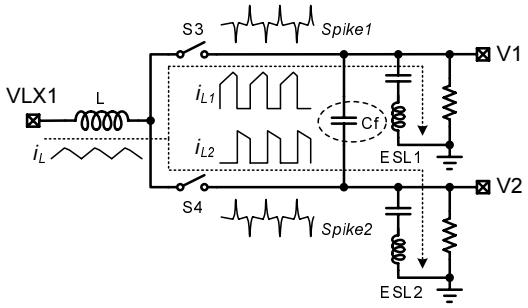

Fig. 5. Output stage structure of SIDO converter with a fly capacitor.

III. System Implementation

Fig. 6 illustrates the system block diagram of a SIDO buck converter with adaptive common-mode control and fly capacitor method. All the power transistors, control circuits and compensation components are monolithically implemented. Average current mode control is adopted in PWM controller to achieve fast response and on-chip compensation. System analysis based on a decoupling small signal model of the SIDO converter has been given in [6]. The inductor current is sensed by filtering the voltage across the inductor [7], which is implemented in the Current Filter block. Zero current detector is adopted in the DCM block to prevent the reverse flow of inductor current.

As shown in Fig. 7, the adaptive common-mode control in Eq. 1 is easy to implement by adding two switches, which are controlled by D_2, at the input of common-mode controller. Compensation design of the common-mode and differential-mode loop is introduced in [6].

In a SIDO converter with PFM control, both D_1 and D_2 are triggered by the comparators of two outputs. Fig. 8 depicts the schematic of the PFM controller. The dcm signal is from the zero current detector, which indicates the converter in DCM state. The on time of D_1 is generated by the delay cell, which is adjusted with the supply voltage and output voltages to limit the output ripples [8]. The converter can automatically switch between PWM and PFM control by the dcm signal instead of accurate load current sensing [9].

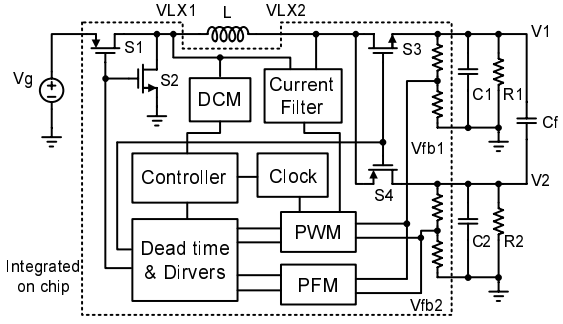

Fig. 6. System block diagram of the proposed SIDO buck converter.

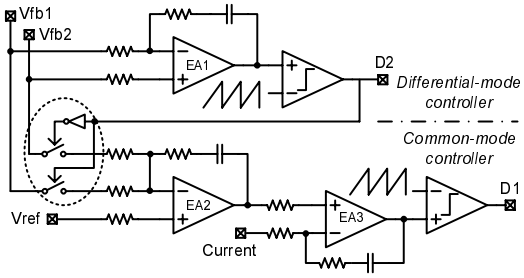

Fig. 7. Schematic of the adaptive common-mode PWM controller.

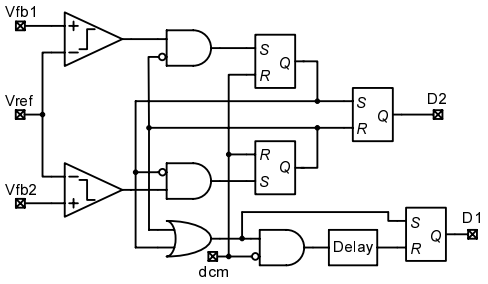

Fig. 8. Schematic of the PFM controller.

IV. Measurement Results

The converter has been fabricated on a 0.25 μm CMOS mixed signal process. The die micrograph is shown in Fig. 9. The chip area is about 2.3 mm $\times$ 2.3 mm with all pads.

Fig. 11 shows the waveform of output ripples and node voltages of $VLX1$ and $VLX2$ without and with the fly capacitor (C_f = 3 μF). It can be observed that the ripples and spikes are nearly half reduced by C_f. The output waveforms in PFM are illustrated in Fig. 12, where C_f reduces the ripples, but also introduces some interaction between two outputs. Load response test (I_1 = 130 mA $\rightarrow$ 400 mA) in Fig. 13(a) shows there is low cross regulation on V_2 and fast response. However, C_f will deteriorate the cross regulation as shown in Fig. 13(b). Fig. 14 illustrates the load response between heavy and light loads (I_1 = 400 mA $\rightarrow$ 33 mA, I_2 = 200 mA $\rightarrow$ 20 mA). The overshot voltage is about 50 mV and response time is less than 20 μs. The conversion efficiency is given in Fig. 10. The SIDO performance is summarized in table 1.

TABLE I
Performance Summary

Process	0.25 μm CMOS	
Chip area	2.3 mm$\times$2.3 mm	
Supply voltage	2.7$\sim$5 V	
Inductor	4.7 μH	
Oscillator frequency	1.3 MHz	
Maximum efficiency	87%	
Output voltages	1.2 V	1.8 V
Filter capacitors	47 μF	47 μF
Load currents	400 mA	200 mA
Output ripples	20 mV	20 mV
Maximum spikes	33 mV	39 mV

V. Conclusion

This paper presents a novel fly capacitor method and adaptive common-mode control for SIDO switching converters. Both PWM and PFM controls are implemented. Measurements on a test chip demonstrate low ripples and spikes, suppressed cross regulations, fast response and improved efficiency. The proposed SIDO converter is suitable for cost-effective power management of portable applications.

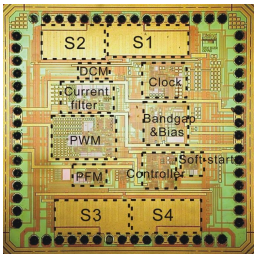

Fig. 9. Chip micrograph.

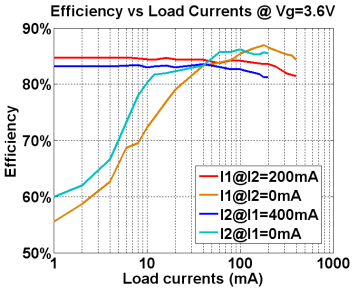

Fig. 10. Power conversion efficiency.

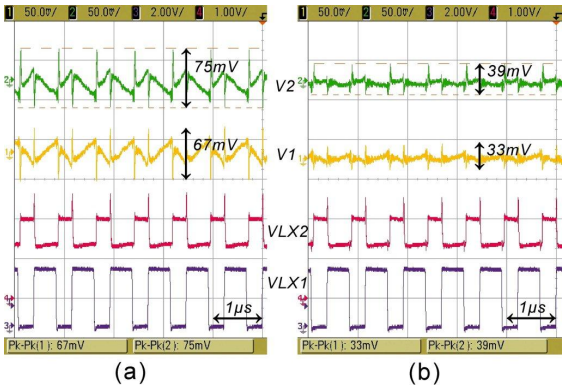

Fig. 11. Measured waveforms of output ripples and node $VLX1$ and $VLX2$ at heavy loads I_1 = 400 mA, I_2 = 200 mA, (a) without C_f, (b) with C_f.

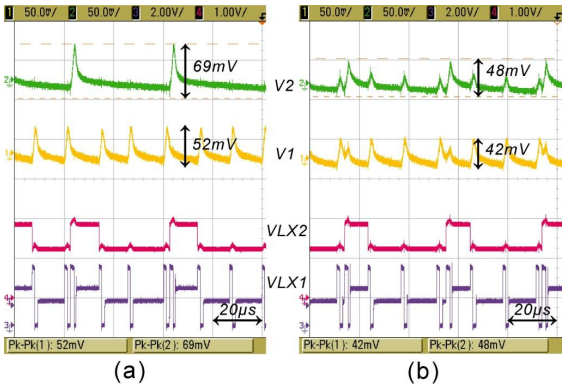

Fig. 12. Measured waveforms of output ripples and node $VLX1$ and $VLX2$ at light loads I_1 = 33 mA, I_2 = 10 mA, (a) without C_f, (b) with C_f.

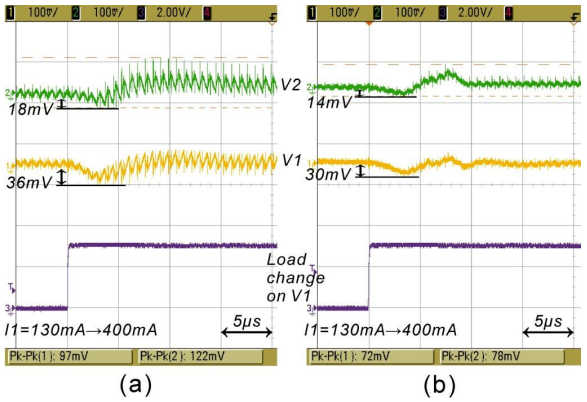

Fig. 13. Load response: I_1 = 130 mA → 400 mA, I_2 = 200 mA, (a) without C_f, (b) with C_f.

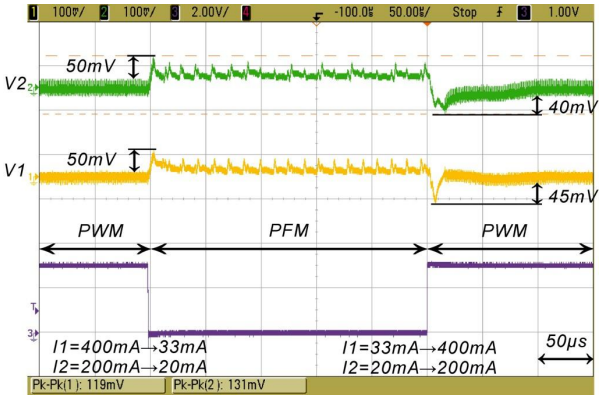

Fig. 14. Load response between PWM and PFM.

References

[1] D. Ma, W.H. Ki, C.Y. Tsui, P.K.T. Mok, "Single-inductor multiple-output switching converters with time-multiplexing control in discontinuous conduction mode", *IEEE J. Solid-State Circuits*, Vol. 38, No. 1, pp. 89-99, January 2003.

[2] D. Ma, W.H. Ki, C.Y. Tsui, "A pseudo-CCM/DCM SIMO switching converter with freewheel switching", *IEEE J. Solid-State Circuits*, Vol. 38, No. 6, pp. 1007-1014, January 2003.

[3] H.P. Le, C.S. Chae, K.C. Lee, etc., "A single-inductor switching DC-DC converter with five outputs and ordered power-distributive control", *IEEE J. Solid-State Circuits*, Vol. 42, No. 12, pp. 2706-2714, December 2007.

[4] D. Trevisan, P. Mattavelli, P. Tenti, "Digital control of single-inductor dual-output DC-DC converters in continuous conduction mode", *IEEE 36th Power Electronics Specialists Conference*, pp. 2616-2622, 2005.

[5] M. Belloni, E. Bonizzoni, etc, "A 4-Output single-inductor DC-DC buck converter with self-boosted switch drivers and 1.2A total output current", *IEEE ISSCC Dig. Tech. Papers*, pp. 444-445, 2008.

[6] W. Xu, X. Zhu, Z. Hong and D. Killat, "Design of single-inductor dual-output switching converters with average current mode control", *IEEE Asia Pacific Conference on Circuits and Systems*, pp. 902-905, 2008.

[7] E. Dallago, M. Passoni, and B. Sassone, "Lossless current sensing in low-voltage high-current DC/DC modular supplies", *IEEE Trans. Industrial Electronics*, Vol. 47, No. 6, Dec. 2000.

[8] B. Sahu, G. A. Rincon-Mora, "An accurate, low-voltage, CMOS switching power supply with adaptive on-time PFM control", *IEEE Trans. Circuits and Systems-I*, Vol. 54, No. 2, pp. 312-321, Feb. 2007.

[9] F. Ma, W. Chen and J. Wu, "A monolithic current-mode buck converter with advanced control and protection circuits", *IEEE Trans. Power Electronics*, Vol. 22, No. 5, pp. 1836-1846, Sep. 2007.