Design of Single-Inductor Dual-Output Switching Converters with Average Current Mode Control

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***Abstract*— An average current mode controlled single-inductor dual-output (SIDO) buck converter is presented. The outputs are specified with 1.2 V/400 mA and 1.8 V/200 mA. The proposed decoupling model helps to analyze the multi-loop system and to design the on-chip compensators. The converter has been fabricated in 0.25-μm mixed-signal process. Simulation and measurement results confirm the proposed analysis. The power efficiency is 86% at a total output power of 840 mW while the output ripples are about 40 mV at an oscillator frequency of 600 KHz.**

I. Introduction

Nowadays there are always different supply voltages required for different functional modules in electronic systems. An interesting and efficient way is to use one converter with a single inductor to generate multiple outputs, which reduces the external components and saves cost and volume.

In recent years, there have been several kinds of single-inductor multiple-output (SIMO) switching converters reported. The converters in [1] and [2] take use of time-multiplexing control, which can be seen as a combination of two independent discontinuous conduction modes (DCM). These converters suffer from very large current ripples and dissipate energy during the freewheeling state. The converter in [3] employs the ordered power-distributive control which has a main channel for compensation and other sub-channels controlled just by comparators. This simplifies the control loop, but has higher ripple and is only suited for small load currents. The solution in [4] adopts digital control for a separate regulation of common-mode and different-mode output voltages. The cross regulation problem is partially compensated by sophisticated control schemes. However, due to the limitation of digital control, the dynamic performance of the converter cannot be satisfying.

This paper presents the analysis and design of an average current mode controlled SIDO buck converter. Section II introduces the system architecture and control sequence. In section III the decoupling model is proposed and the stability problem is investigated. The measurement results in section IV will confirm the system analysis. A brief conclusion is given in section V.

II. Architecture of SIDO buck converter

Fig. 1 illustrates the architecture of a SIDO buck converter with average current mode control. It can be seen that two power switches SW3 and SW4 are added to obtain two outputs, which is different from the single-output converter. There are two main control loops: one is the common-mode loop, which regulates the total energy by controlling the input switches SW1 and SW2, and the differential-mode loop, which determines the distribution of inductor current between two output channels by controlling the output switches SW3 and SW4.

The converter is designed for an output load of 400 mA at 1.2 V on the first channel and 200 mA at 1.8 V on the second with an input voltage ranging from 2.8 V to 5 V. The off-chip inductor is 4.7 μH and the filter capacitors are 22 μF. All compensation components are implemented on-chip.

The control sequence is shown in Fig. 2. The duration of

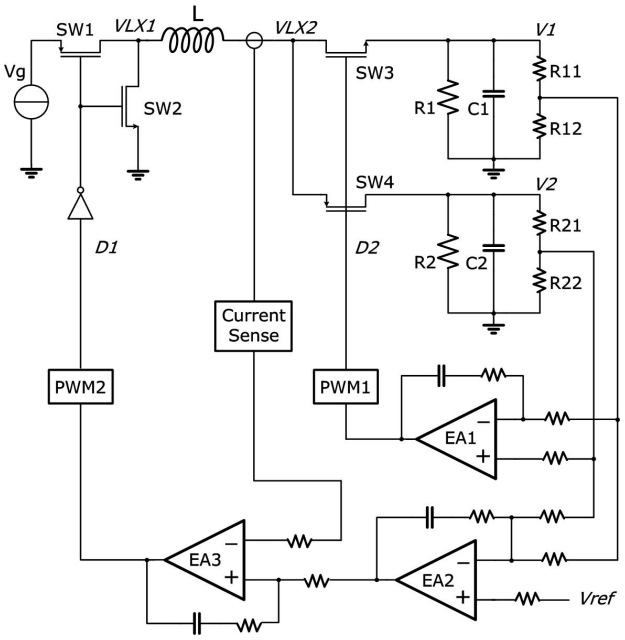

Fig. 1. System architecture of the average current mode controlled SIDO buck converter.

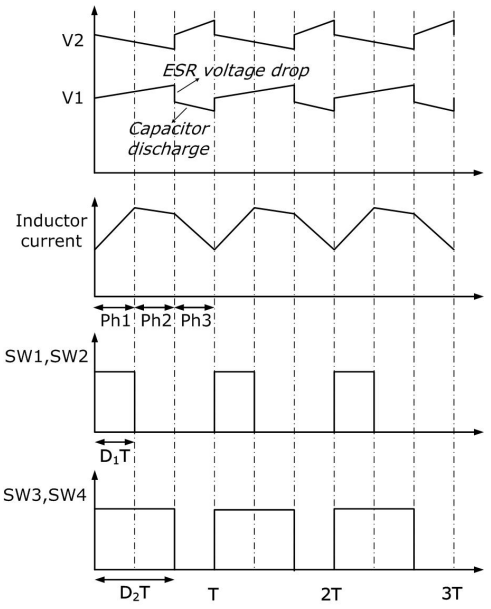

Fig. 2. Control sequence and output ripples.

duty-cycle D_2 is adjusted according to the ratio of two load currents. The waveforms of the steady-state inductor current and output voltage ripples in continuous conduction mode (CCM) are also depicted. According to Fig. 2, the ripples of SIDO output voltage mainly consist of two parts: the charge and discharge of capacitors and the voltage drop on the equivalent series-resistor (ESR) of capacitor. If the current ripple of the inductor is neglected, the output ripples in CCM can be estimated as:

$$V_{ripple1} = \frac{(1-D_2)I_1}{fC_1} + I_L R_{ESR1} \tag{1}$$

$$V_{ripple2} = \frac{D_2 I_2}{fC_2} + I_L R_{ESR2} \tag{2}$$

where f is the switching frequency. So, the steady-state voltage ripples depend on the discharging time and inductor current when switching SW3 and SW4. DCM and Pseudo-CCM control in [1] and [2] have longer discharging time and higher peak current, thus have larger ripples.

III. Design of SIDO buck converter

The switching converter works as a feedback controlled system so that the stability and dynamic response are the key problems in converter design. In this section the small signal model of SIDO power stage is derived. The research is focused on the decoupling analysis of the multi-loop system. Based on the decoupling model, the procedure for the compensator design is derived.

A. Small Signal Model

Assuming the ripples and ESRs are negligible, the small signal behavior of the power stage can be described by state space equations as:

$$\frac{d}{dt}\begin{bmatrix}\hat{v_1}\\ \hat{v_2}\\ \hat{i_L}\end{bmatrix} = \begin{bmatrix}-\frac{1}{R_1C_1} & 0 & \frac{D_2}{C_1}\\ 0 & -\frac{1}{R_2C_2} & \frac{1-D_2}{C_2}\\ -\frac{D_2}{L} & \frac{1-D_2}{L} & 0\end{bmatrix}\begin{bmatrix}\hat{v_1}\\ \hat{v_2}\\ \hat{i_L}\end{bmatrix} + \begin{bmatrix}0 & \frac{I_L}{C_1}\\ 0 & -\frac{I_L}{C_2}\\ \frac{V_g}{L} & \frac{V_2-V_1}{L}\end{bmatrix}\begin{bmatrix}\hat{d_1}\\ \hat{d_2}\end{bmatrix} \tag{3}$$

$$\begin{bmatrix}\hat{v_{CM}}\\ \hat{v_{DM}}\\ \hat{i_L}\end{bmatrix} = \begin{bmatrix}m_1 & m_2 & 0\\ m_1 & -m_2 & 0\\ 0 & 0 & 1\end{bmatrix}\begin{bmatrix}\hat{v_1}\\ \hat{v_2}\\ \hat{i_L}\end{bmatrix}$$

whereas the feedback coefficients are $m_1 = R_{12}/(R_{11}+R_{12})$ and $m_2 = R_{22}/(R_{21}+R_{22})$.

The SIDO converter in Fig. 1 is a multi-loop system which has several cross-regulated complex blocks. It is necessary to consider the whole small signal structure as shown in Fig. 3 when dealing with the stability problems.

In Fig. 3, the transfer functions $G_{11}(s)$, $G_{21}(s)\cdots G_{32}(s)$ can be derived from (3). According to the system architecture of Fig. 1, $G_{PWM1}(s)$ and $G_{PWM2}(s)$ are the transfer functions of pulse-width modulation (PWM) signal generators. $G_{DM}(s)$ stands for the proportion-integration (PI) controller EA1 of Fig. 1 in the differential-mode loop. $G_v(s)$ represents the PI controller EA2, $G_i(s)$ the transfer function of sensing the inductor current and $G_c(s)$ the controller EA3 in the common-mode loop. The complexity of the SIDO system lies on the multi-loop feedback control property. It is feasible to decompose the system into several single-loop sub-systems

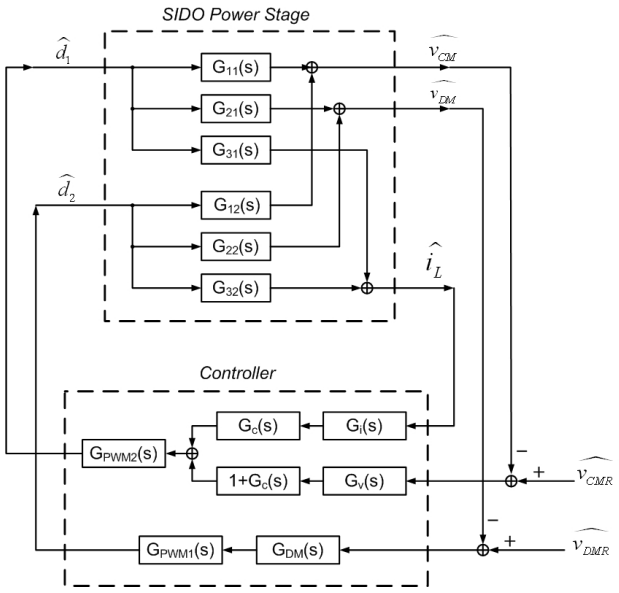

Fig. 3. Small signal structure of the SIDO system.

which have the same stability characteristics. Thus, the SIDO system can be decoupled into differential-mode and common-mode sub-systems to solve the stability problem.

B. Differential-mode Sub-system

When the common-mode loop is closed, the inductor behaves as a current source because of the average current mode control. Therefore, the approximated transfer function from $\hat{d_2}$ to $v_{\hat{DM}}$ can be expressed as:

$$F_{DMa}(s) = I_L(\frac{m_1 R_1}{1+sR_1C_1} + \frac{m_2 R_2}{1+sR_2C_2}). \quad (4)$$

Eq. (4) give us the valuable information that the power stage of the differential-mode works as a first-order system whose dominant pole is related to the output capacitors and resistors. Based on it, the compensator of EA1 can be designed properly. Because of on-chip compensation, the zero of the PI controller is higher than the pole of power stage. Therefore, large gain is needed to make the crossover frequency much higher than the zero. On the other hand, the maximum gain of $G_{DM}(s)$ at the switching frequency is limited by the ramp slope of the saw-tooth waveform to avoid sub-harmonic oscillation problems.

$$|G_{DM}(s)|_{\omega=2\pi f} < \frac{V_{saw} f C_1}{(m_1+m_2)I_1} \quad (5)$$

where V_{saw} is the amplitude of the saw-tooth waveform. Eq. (5) decides the ratio of resistors in the compensator.

The bode plot of the periodic AC (PAC) simulation in Spectre is shown by the dashed line in Fig. 4, which demonstrates the phase margin of 85 degree and the crossover frequency of 145 KHz. According to the bode plot in Fig. 4, the loop gain is important for stability and response.

C. Common-mode Sub-system

When the differential-mode loop is closed, according to the small signal equation (3) and Fig. 3, the approximated transfer function from $\hat{d_1}$ to $\hat{i_L}$ and $v_{\hat{CM}}$ is given by:

$$F_{CMia}(s) = \frac{V_g}{sL + \frac{D_2^2 R_1}{1+sR_1C_1} + \frac{(1-D_2)^2 R_2}{1+sR_2C_2} + R_{eq}} \quad (6)$$

$$F_{CMva}(s) = [\frac{m_1 D_2 R_1}{1+sR_1C_1} + \frac{m_2(1-D_2)R_2}{1+sR_2C_2}]F_{CMia}(s) \quad (7)$$

with $R_{eq} = \frac{V_2 - V_1}{I_L}\frac{m_1 D_2 - m_2(1-D_2)}{m_1+m_2}$.

Eq. (6) and (7) show that the power stage of the common-mode sub-system behaves as a normal buck converter with the resonance frequency $\omega = \sqrt{\frac{D_2^2+(1-D_2)^2}{LC}}$.

Based on this conclusion, the compensation of the common-mode sub-system can be designed. Average current mode control is adopted to achieve good stability, fast response and noise immunity. The design of current mode control has been studied in many literatures [5], [6]. The configurations of the current loop and the voltage loop have been discussed in [7]. Here the outer loop transfer function of common-mode in Fig. 3 is written as:

$$H_{CMout}(s) \approx \frac{F_{CMva}(s)F_v(s)}{1+F_{CMia}(s)F_i(s)}. \quad (8)$$

where $F_v(s) = G_v(s)(1+G_c(s))G_{PWM2}(s)$, $F_i(s) = G_i(s)G_c(s)G_{PWM2}(s)$.

Fig. 5 gives the outer loop simulation of the common-mode sub-system with current loop closed, which shows the phase margin of 52 degree and the crossover frequency of 120 KHz.

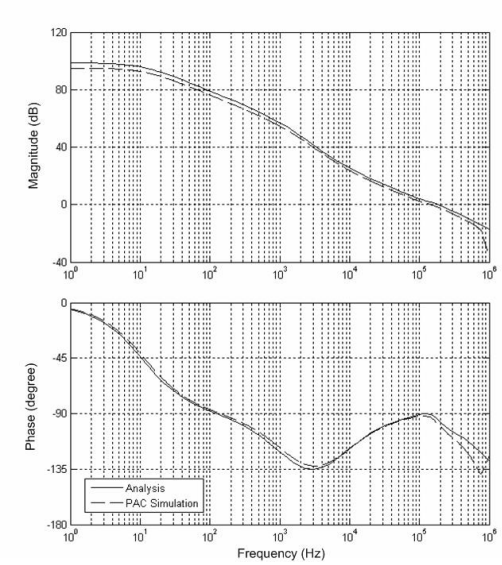

Fig. 4. Bode plots of the differential-mode sub-system.

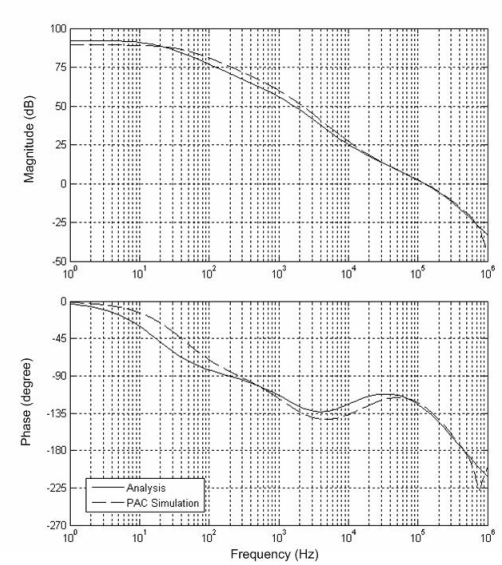

Fig. 5. Bode plots of the outer loop in the common-mode sub-system.

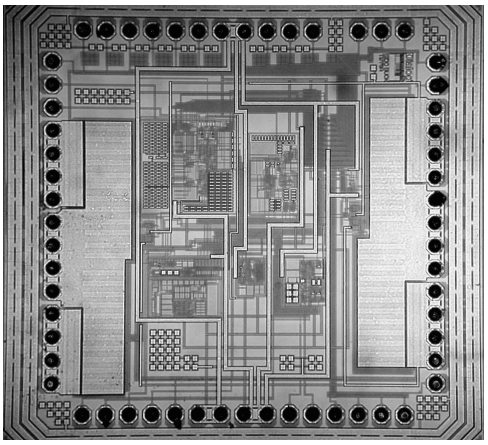

Fig. 6. The die micrograph of the SIDO converter.

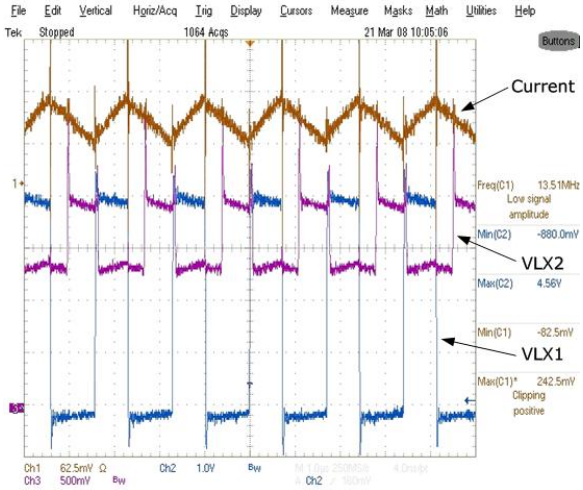

Fig. 7. Waveforms of the inductor current, node VLX1 and VLX2.

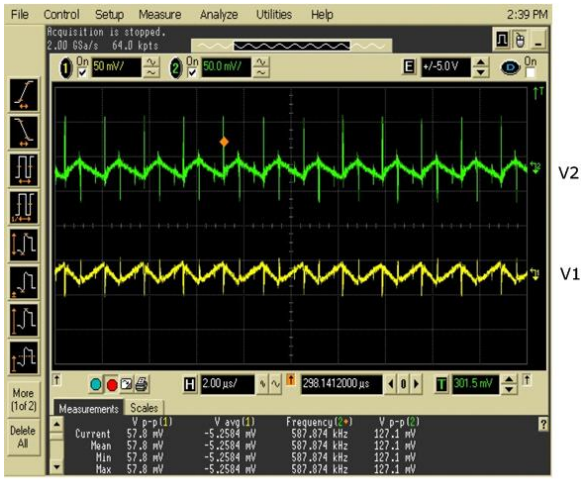

Fig. 8. Ripples of two output voltages.

TABLE I
SIDO PERFORMANCE SUMMARY

Process	TSMC 0.25 μm, 1P4M	
Chip area	2.2 mm$\times$2.2 mm	
Supply voltage	2.8$\sim$5 V	
Inductor	4.7 μH	
Oscillator frequency	600 KHz	
Maximum efficiency	95%	
Output voltages	1.2 V	1.8 V
Load currents	400 mA	200 mA
Filter capacitors	22 μF	22 μF
Output ripples	40 mV	40 mV
Maximum spikes	50 mV	100 mV

IV. MEASUREMENT RESULTS

The SIDO converter has been implemented with 0.25 μm mixed-signal process. The micrograph is shown in Fig. 6. When $V_g = 4$ V, $R_1 = 3\ \Omega$, $R_2 = 9\ \Omega$, the waveforms of the inductor current and the node VLX1 and VLX2 are illustrated in Fig. 7. So, the converter works stably without any subharmonic oscillation. The spikes on node VLX2 result from the dead-time control of SW3 and SW4. Fig. 8 shows the waveform of the ripples of two outputs, which correlates well with that in simulation. It can be observed that the ripples are about 40 mV at the frequency of 600 KHz. There are some spikes which are caused by the equivalent series inductor (ESL) of the filter capacitors. The efficiency at full load is 86%. And the maximum efficiency reaches 95% under the load condition $I_1 = 10$ mA, $I_2 = 148$ mA. The performance of the converter is summarized in table I.

V. CONCLUSION

This paper presents an average current mode controlled SIDO buck converter. The system stability was investigated and the decoupling analysis of this multi-loop system was proposed. Simulation results have verified the system analysis. Measurements on a test chip demonstrate low ripples and high efficiency. The SIDO converter is suitable for cost-effective power management of portable electronics.

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