A Capacitive Step-Down Converter Using a Linear Mode Pre-Regulator for Improved Load Regulation

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Abstract

A capacitive step-down converter in 0.25 µm CMOS using a linear mode pre-regulator is presented. The linear pre-regulator operates both in pulse frequency mode under low load conditions and in current mode under high output load. In pulse frequency mode the pre-regulator limits the charge current of the capacitor network improving the electromagnetic compatibility. Under high load conditions the converter operates in a current mode which means that the switched capacitors are clocked with a fixed duty cycle ratio and the regulation of the output voltage is performed by the pre-regulator.

1. Introduction

Capacitive step-down DC-DC converters are advantageous for low cost applications like CD-players or MP3-players where energy efficient step-down conversion is required and cost requirements are predominant. A drawback of capacitive converters compared to converters with inductance is possibly the high-frequency radiation and low frequency interference. Both the input current spike and the discharge current impact the EMC [1]. Also the PWM is not very suited for SC step-down converters because of the nonlinear charge transfer characteristics of the RC network.

In this paper we present a new approach for the regulation of a capacitive step-down converter that uses a linear mode transistor in front of the capacitive divider. The converter has a variable transfer ratio of 1:1, 3:2 and 2:1 allowing an input voltage of 2.8 to 5 V for an output load of 200 mA at 1.8 V. The selected process is 0.25 µm CMOS with 5V/2.5V option.

Section 2 discusses the output voltage ripple. Section 3 describes the small signal characteristics. Section 4 and 5 present the fabricated test circuitry.

2. Output Ripple with Pre-Regulator

The principle of the converter is shown in Fig. 1. The pre-regulator can be considered as a current source that charges the transfer capacitors $C_{t,1}$ = 1µF and $C_{t,2}$ = 1µF using the switches S5 and S7. Under high load conditions the charge pump is operated in a so called "current mode", this means the SC network is running with a fixed duty cycle ratio, which makes the smallest output voltage ripple, and the output voltage is regulated by the controlled current source I_{ch}. Under low load conditions, this means below 10 % of the maximum load, the maximum load current of source I_{ch} is fixed and the output voltage V_L is regulated by pulse skipping (PFM).

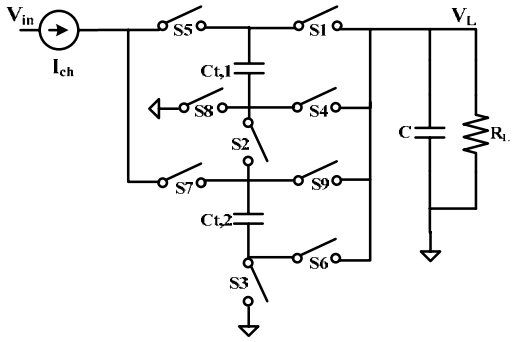

Figure 1. Charge pump and current source input.

Table.1. Switch sequences of the charge pump.

Ratio	Phase.1	Phase.2	Off
1/2	4, 5, 6, 7	1, 3, 8, 9	2
2/3	4, 5, 6, 7	1, 2, 3	8, 9
1	Always On: 1, 3, 5, 8, 9		2, 4, 6, 7

The ripple in current mode (CM) and PFM can be calculated by solving the steady-state equations [2]:

$$\begin{cases} \dot{X} = AX + BU \\ \dot{Y} = CX + DU \end{cases}$$

with

$X = \begin{bmatrix} V_t & V_C \end{bmatrix}^T$, $Y = \begin{bmatrix} V_L \end{bmatrix}$, $U = \begin{bmatrix} I_{ch} \end{bmatrix}$.

V_t is voltage on the transfer capacitor, V_C the voltage of the output capacitor C = 4.7 µF, I_{ch} the charging current.

After some calculations we can show that the output voltage and the output voltage ripple can be expressed as:

$$V_L \approx V_C = \frac{n}{n-1} d I_{ch} R_L \qquad (1)$$

$$V_{L,ripple} \approx \begin{cases} \left| \frac{n-1}{n} - d \right| \frac{V_L}{R_L} \left(\frac{1}{f \cdot C} + \frac{R_{ESR}}{d(1-d)} \right) & d \neq n-1/n \\ R_{ESR} \frac{V_L}{f \cdot R_2 \cdot R_L} \frac{n-1}{nC_t} & d = n-1/n \end{cases} \quad (2)$$

The duty ratio is d, the transfer mode is n = 2 in the 1:2-mode and n = 3 in the 2:3-mode. R_{ESR} belongs to the output capacitor, R_2 is the discharge resistance. In 1:1-mode the circuit works like a linear voltage regulator. For lowest ripple in current mode d is set to (n-1)/n.

Fig. 2 depicts the calculated efficiency and ripple versus load current for both modes of operation, the current mode (CM) and the pulse skipping mode (PFM). For load currents above 20 mA we choose the current mode, because the loss in efficiency is only about 4 % compared to the 71 % efficiency in PFM, but the theoretical ripple is only a few mV compared to over 20 mV in PFM.

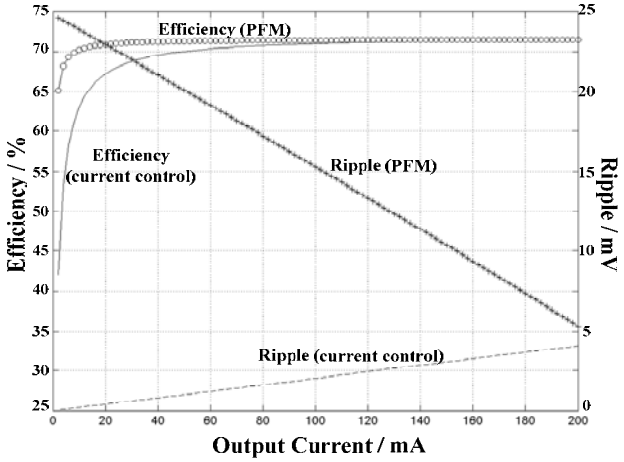

Figure 2. Efficiency and ripple of charge pump in current mode (CM) and pulse skipping mode (PFM).

3. Stability Considerations of Regulation Loop

The loop of a capacitive step-down converter is easier to compensate as the loop of an inductive converter: The inductor impedance and the storage capacitor make a 2nd order system requiring the regulation of the average current flowing through the inductor to become stable. Hence inductive converters need a precise current sense. Our capacitive converter also has a current sense, but it is less critical, because it is only used to control between the current mode and pulse skipping mode and to fine adjust the levels of the charge pump transfer ratios.

The small signal model of the loop when operated in current mode is depicted in Fig. 3 [3]. The difference of the target value V_{ref} and the error signal from the resistive divider $K_r=R_{1L}/(R_{1L}+R_{2L})$ multiplied with the transfer function of the error Amplifier $A_{ea}(s)$ sets the control voltage $V_{control}(s)$ for the pre-regulator PMOS transistor. The V_{GS} for the pre-regulator PMOS, the charge voltage $V_{ch}(s)$, is the difference of input voltage $V_{in}(s)$ and the control voltage $V_{control}(s)$. The conductance G_m of the pre-regulator supplies the SC-network (charge pump) with a charge current $I_{ch}(s)$. The impedance of the SC-network including the load is $R_{cp}(s)$. The load is composed of the capacitor C_L and its resistance R_{ESR}, and the load resistor R_L.

The open loop transfer function is:

$$G_{OL}(s) = K_r \cdot G_m \cdot R_{cp}(s) \cdot A_{ea}(s) \quad (3)$$

The dominant pole is defined by the load:

$$p_1 \approx \frac{1}{CR_L} \Big/ \left(1 + \frac{C_t}{(n-1)C} \right) \quad (4)$$

The second and third pole result from the error amplifier and the discharge resistor R_2 of the SC-network:

$$A_{ea}(s) = \frac{A_e}{(1+s/p_{e1})(1+s/p_{e2})} \quad (5)$$

$$p_2 \approx \frac{(n-1)(1-d)}{C_t R_2} \cdot \left(1 + \frac{C_t}{(n-1)C} \right) \quad (6)$$

The dominant pole $p_1 = 3.1$ kHz is defined by the load resistor $R_L = 9\ \Omega$ and the output capacitor $C = 4.7\ \mu F$. The 2nd and 3rd pole are at 40 kHz and 100 kHz. A compensations circuit comprising a voltage controlled voltage source injects a current $i(s) = s\, C_c\, V_L(s)$ into node A (Fig. 3) to generate a LHP zero $Z_c = 1 / (C_c\, R_{2L})$. This compensates the 2nd pole and improves stability.

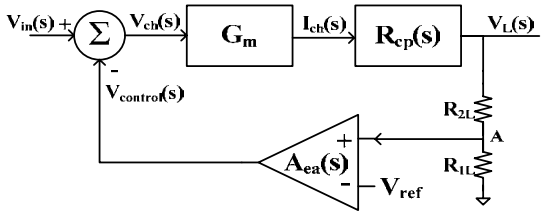

Figure 3. Small signal model of loop.

4. System Overview

Fig. 4 gives an overview of all functions implemented on the test chip. The input voltage is sensed and compared to a reference that is composed of the bandgap reference and a control signal from the current sense. The comparator outputs set the transfer ratio of the charge pump, the output current sense sets the operation modes (current mode or PFM). The pre-regulator PMOS (Pass Transistor) is either controlled by the current control, when the PMOS is part of the regulation loop, or it is controlled from block "Pulse Frequency Modulation" that sets the V_{GS} of the Pass Transistor to a fixed value. The test chip comprises all functions required to operate the converter stand-alone, these are a bandgap reference and an on-chip oscillator. The output current sense is realized by current mirroring the Pass Transistor.

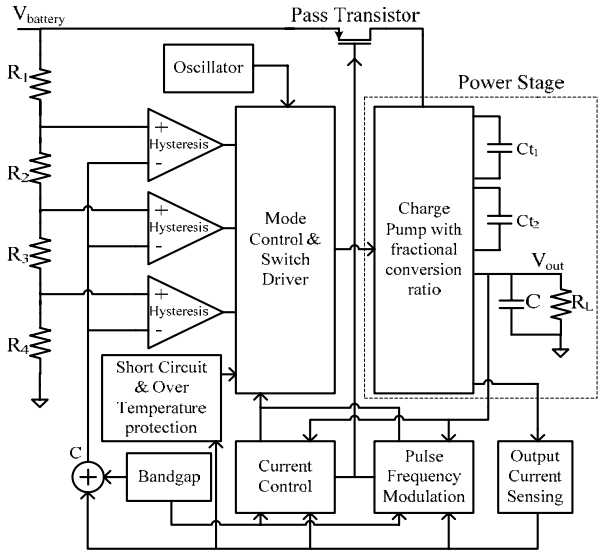

Figure 4. System block diagram.

5. Test Chip and Measurements

The test chip is implemented using a 0.25 µm 2-Poly 4-Metal CMOS process with a die size of 1.7 mm × 2.0 mm including the pad ring (see Fig. 5). The test circuit comprises special test modes and test interfaces allowing detailed analysis of the system blocks (Fig. 4). The microphotograph shows the bond-version of the TSSOP-28 package for access of test interface. A second version assembled in a MLPD-8 package is pin compatible to standard applications.

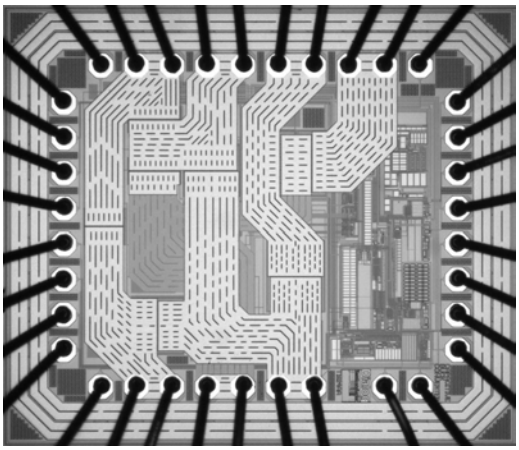

Figure 5. Chip microphotograph.

The converter has 2 operation modes, the current mode (CM) with load currents above 20 mA, and the burst mode (PFM) with load currents below 20 mA. An important issue is the efficiency of the converter under low load and high load current conditions. Fig. 6 shows the summarized efficiency measurement results. At high input voltages (5 V) we have a 2-to-1 capacitor ratio. The efficiency increases when the input voltage decreases down to 4 V. Below 4 V input the converter switches to 3-to-2 mode. The 1:1 mode is entered for input voltages below 3.2 V. The highest efficiency is achieved for the lowest input voltage of the 2-to-1 mode, this is at 4.2 V, the lowest efficiency occurs for low load current when the 1-to-1 mode is entered. In that case the efficiency is similar to that of a simple linear voltage regulator.

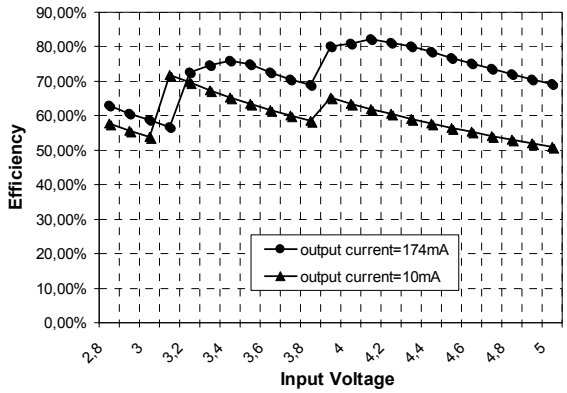

Figure 6. Efficiency versus input voltage.

6. Conclusions

A new approach for capacitive step-down converters that use a linear mode pre-regulator for improved load regulation is discussed. The pre-regulator replaces the pulse width modulation or pulse skipping regulation of conventional capacitive step-down converters by an operation mode called “current mode” with a fixed duty cycle which minimizes the output voltage ripple. Under low load conditions the pre-regulator reduces the maximum load current of the SC network at the input node which also reduces peak currents and improves the EMC.

References

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