A Sub-1-V CMOS Bandgap using Forward Body Bias of the PMOS Differential Pair for Reduction of the Threshold Voltages

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Abstract

A low voltage bandgap for 180 nm and 130 nm CMOS processes using standard threshold transistors and a forward body bias technique of the PMOS differential input pair is presented. The bandgap uses the current mode approach to generate a reference voltage below the silicon bandgap. The source-bulk-junction of the PMOS differential input is forward biased to lower the threshold voltage. The forward biasing switches on the parasitic bipolar comprising source, bulk and substrate, which reduces the bias current of the differential pair. This problem is considered during design and a new circuit is developed that compensates for the reduced bias current by adjusting the load current of the differential stage. The bandgap output voltage is 600 mV and consumes a supply current of only 9.5 µA.

1. Introduction

Low voltage references get more attention whereas the core voltage supply of deep submicron technologies fall below the 1-V border. In battery supplied applications for mobile electronics the supply voltage must be carefully monitored, as the mobile electronics uses complex power management schemes to enhance operating and stand-by time. From a system point of view it would be advantageous to have a supply monitor running on the lowest supply voltage that is used in a mixed signal system, because this would be the first supply domain that is powered up during startup, and would the supply domain powered down at last during shut down.

CMOS technologies with supply voltages from 1 V to 1.5 V feature several options for the threshold voltages (V_{TH}) that would allow implementation of low voltage circuitry using low V_{TH} on the one hand, and high V_{TH} on the other hand where speed is less important than static power consumption. For battery operated systems the standby current that is measured in units of µA is affected by the leakage, hence medium and high threshold transistors are prefered in low power applications. Furthermore the low V_{TH} transistors require additional masks which means costs, and are likely to be left in the processing. This gives the scope of application for low voltage bandgaps using standard V_{TH} transistors.

2. Forward Biasing the Source-Bulk Junction

For low voltage analog design several approaches are discussed [1]. The forward body bias technique of the source-bulk junction is discussed in a few applications either with very low currents that allow to neglect the parasitic collector currents and the reduced tail current of the differential pair [2], or the bias is accomplished by a very low fixed voltage of e.g. 0.3V avoiding significant parasitic junction currents [3]. Forward bias by using a current across the junction has the advantage that it can be used at variable source potentials, e.g. for differential input stages. Forward biasing the source-bulk junction with a fixed voltage over the full temperature range would lead to temperature dependant parasitic substrate current. The temperature dependant parasitic current is not a problem if the source is connected to VDD [2].

The schematic of a PMOS transistor with source-bulk junction and parasitic bipolar transistor is indicated in Fig. 1a. The standard Spice model of a PMOS includes the source-bulk diode, but not the parasitic bipolar and the resulting collector current if the source-bulk junction is forward biased. For modelling the collector current the intrinsic PMOS model is used plus an additional transistor Q, as shown in Fig. 1b. The forward bias current flows through the voltage source Vmeas, that has 0 V and is only used to measure the current for the current controlled current source I(Vmeas). The source-bulk diode D_{SB} sets the source-bulk voltage V_{SB}. The additional current flowing into the substrate is modelled by the bipolar Q that is biased by I(Vmeas).
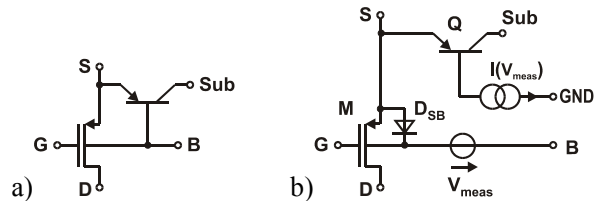

Figure 1: a) PMOS with parasitic bipolar transistor, b) simulation model

The total additional current I_{SB} that is pulled out of node S is:

$$I_{SB} = I(D_{SB}) + I_{Q,E} = I_B + (\beta + 1)\,I_B = (\beta + 2)\cdot I_B$$

The current I_{SB} is not exact as it is too high by $1\cdot I_B$, also the parasitic capacitance is not exactly modelled. The

error in current can be compensated by feeding a current I_B into node S using an additional current source not drawn in Fig. 1b. The redundant source node capacitance can be removed by disconnecting the bipolar emitter from node S using an additional controlled current source pulling the emitter current out of node S.

The parasitic bipolar has a bias and temperature dependant current gain β between 2.5 at −25°C and a maximum β of 6 at + 125°C. The temperature coefficient of V_{BE} in the process used is about −1.9 mV/°C. Already with a low base current of 15 nA we get a V_{BE} of 680 mV at room temperature with an emitter area $A_E = 2\mu m^2$.

3. Temperature Characteristics of Threshold Voltage

The absolute value of the threshold of the PMOS transistors decreases with increasing temperature. For a device with W/L = 10 μm / 0.5 μm, $V_{DS} = 100$ mV and $I_{DS} \approx 10$ μA, the TC of the treshold is about + 0.8 mV/°C.

Both absolute values of the diode voltage and the threshold of the PMOS decreases with increasing temperature. This has a very interesting effect as can be seen in Fig. 2: The lower curve is the threshold without forward body bias, the upper curve the threshold with a body bias voltage of a diode with 15 nA bias current. The forward body bias voltage increases at lower temperatures, increasing the body effect and leading to stronger threshold reduction. The resulting threshold (upper curve in Fig. 2) has a low temperature coefficient. The temperature stabilized threshold of the differential input is very beneficial for low voltage circuit design regarding the saturation margin and the reduced temperature sensitivity of channel leakage current.
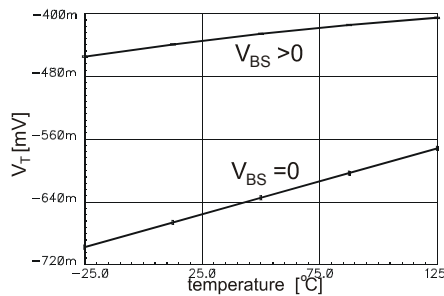

Figure 2: Threshold versus temperature of a PMOS (W/L=10/0.5 μm), $I(D_{SB})$ = 15nA.

4. Differential Input Pair and Monitor Stage

The principle of the differential input pair with forward biased source-drain diode and the parasitic bipolars is shown in Fig. 3. The emitter current drawn from the tail current is not an exact value and varies with the

temperature characteristic of β. Hence the load current biasing must be adjusted to match the reduced tail current and the temperature sensitive and process variable drain current.
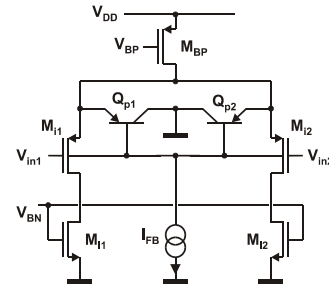

Figure 3: Differential input with biasing of bipolars.

The bias voltage V_{BN} can be set using a monitor stage. The monitor stage principle is depicted in Fig. 4. A second input stage that can be scaled in transistor dimensions and bias current, is placed in parallel to the main input stage. The monitor stage is a small replica of the main input stage with the purpose to reflect the loss in bias current by the parasitic bipolars. The output of the monitor stage is the tail current minus the current lost by the β of the parasitic bipolars and is fed to the reference transistor M_{LX}. This reference transistor supplies the bias node V_{BN} of the main differential stage.
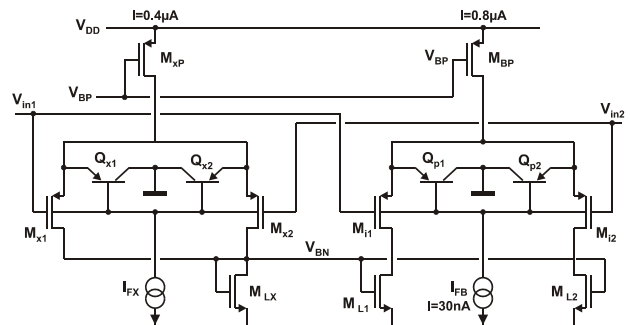

Figure 4: Monitor stage (left) and main input (right).

5. Current Mode Bandgap

The schematic of the current mode bandgap is shown in Figure 5. The principle of the current mode bandgap is described in detail in [3,4]. A large current density ratio of 32 is achieved by using a current mirror ratio of 4 and a bipolar area ratio of 8. At the operating point the voltages V_A and V_B are equal and the PMOS current sources supplies a nearly temperature independent current to the network of bipolar transistors and resistors. The voltages V_A and V_B are divided by 2 (node V_{A23} and V_{B23}) before they are fed to the amplifier input. This gives additional saturation margin to the current source of the PMOS differential pair inside the amplifier. The

amplifier is a folded cascode OTA with common source output stage and an internal compensation. The total open loop gain under worst case conditions is above 90 dB, ensuring sufficient low frequency power supply rejection.
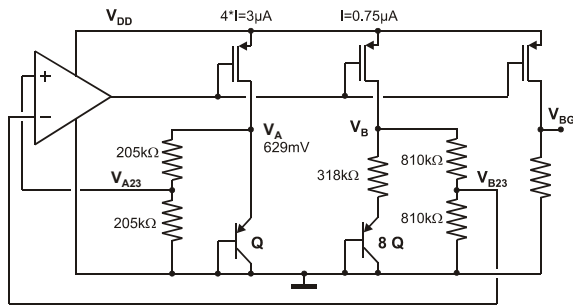

Figure 5: Schematic of current mode bandgap.

6. Test Circuitry and Measurement Results

The chip microphotograph of the test circuitry using a 180 nm standard CMOS process with MIM-capacitors and 6-Metal layers is shown in Fig. 6. Size of the bandgap reference is 410 μm × 210 μm. Most part of the area is consumed by the resistor array, the resistor of the self biasing (not shown in Fig. 5) and the frequency compensation.
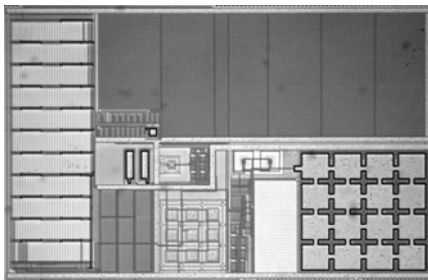

Figure 6: Chip microphotograph.

The output of the bandgap reference versus temperature, shown in Fig. 7, is about 606 mV ± 4 mV for VDD ≥ 1.0 V and tmperatures below 125 °C. At 0.9 V supply the large V_{BE} affects the saturation of the PMOS current sources at low temperatures.
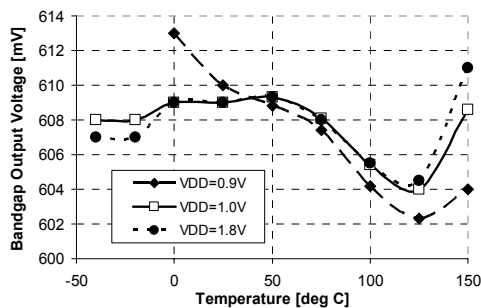

Figure 7: TC of 180nm-CMOS bandgap.

A second version of the bandgap is fabricated on a 130 nm CMOS process. This version shows stable output voltage down to 0.9 V supply, actually at –25 °C. The DC–PSRR is plotted in Fig. 8. As the real V_{BE} deviates from the Spice model, the temperature characteristics of this test circuit is not centered yet.
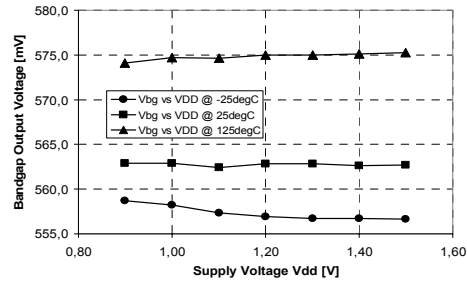

Figure 8: DC–PSRR of 130nm-CMOS Sub-1V Bandgap

7. Conclusions

The forward body bias technique of the source bulk junction of a PMOS differential pair is used in sub-1-V CMOS bandgap references. A monitor stage in parallel to the amplifier input stage measures the current of the parasitic bipolar transistor and adjusts the load current of the main amplifier input stage. The forward bias voltage at room temperature is 680 mV and reduces the threshold of the PMOS transistors about 220 mV.

Two bandgap references using the current mode approach are fabricated, one for a 180-nm and one for a 130-nm CMOS process. The lowest supply voltage is restricted by the reference diode voltage at low temperatures plus the saturation voltage of the PMOS current source connected to the reference diode.

References

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