

# One-Chip Solution in 0.35 $\mu\text{m}$ Standard CMOS for Electronic Ballasts for Fluorescent Lamps

Dirk Killat, Joachim Schmidt, Andreas Baumgaertner,  
Robert Baraniecki, Oliver Salzmann,  
Dialog Semiconductor GmbH, Kirchheim-Teck, Germany,  
dirk.killat@diasemi.com

## Abstract

*An ASIC for full digital control of electronic ballasts for fluorescent lamps is presented. The one-chip solution is the functional integration of 3 chips, an IC for the PFC, a lamp management ASIC and a half bridge driver IC. The ASIC has 3 V compatible high precision ADC and comparator inputs, a fully digital controlled PFC, a digital regulation of the lamp power and a state machine establishing the lamp management. The outputs are 13 V high speed FET drivers that are directly controlled by the digital logic. The paper presents the topology of the electronic ballast, the interfaces to the two main control loops, and the main analog and digital blocks. The ASIC is fabricated in a 0.35  $\mu\text{m}$  standard CMOS process. The system building blocks and the topology can be used for various highly integrated power electronics applications.*

## 1. Introduction

The one-chip solution for electronic ballasts for fluorescent lamps is the integration of the functionality of 3 integrated circuits: 1st is the power factor corrector (PFC) standard IC, fabricated in 400 V compatible BCD technology and an analog regulation of the PFC. 2nd is a full custom ASIC in a 0.7  $\mu\text{m}$  CMOS process [1], with analog regulation of the lamp power and digital lamp management. 3rd is a half bridge driver standard IC that establishes the high site and low site driver for the output.

The integration of all functions opens the question which technology should be used. The most popular approach is choosing a high voltage compatible BCD technology that makes it easy to design interfaces to the power electronics environment. A disadvantage is the low digital integration capability of these processes that make high integrated systems on chip difficult to realize from a commercial point of view. Our approach is a SoC-ASIC solution using a standard 0.35  $\mu\text{m}$  CMOS process. All inputs to the SoC-ASIC are voltage limited, the outputs are compatible with the gate driving voltage of external

power FETs. This strategy will require some additional discrete components, but it opens the chance for a high integrated SoC in a power electronics environment.

## 2. Electronic Ballast Principle

The principle of the electronic ballast is shown in Fig. 1. The mains supply is rectified and fed to a boost converter (PFC). The boost converter makes a sinusoidal current, this means the input current is proportional to the input voltage and therefore provides a powerfactor of nearly 1. The transformed energy is fed to a storage capacitor that supplies the load during zero crossing of the input AC voltage. A typical storage capacitor voltage  $V_{\text{bus}}$  is 400 V, that is above the maximum rectified AC mains supply. Hence the PFC is working as a boost converter. The energy storage supplies the half bridge, comprising 2 external NMOS power FETs in push-pull configuration and an auxiliary circuit with a small transformer to drive the high site gate. The lamp power is frequency controlled, therefore an inductive impedance with a DC decoupling capacitor is in series with the fluorescent lamp. Typical frequencies of operation are above 40 kHz.

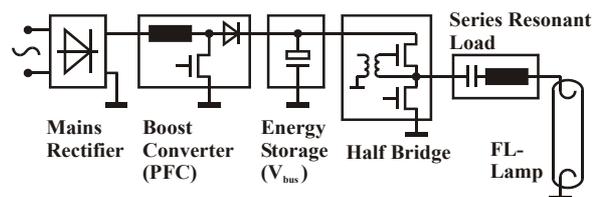


Fig. 1. Electronic Ballast Principle

The described system has two sections that have to be controlled by the SoC-ASIC. One is the input section comprising the mains supply, the boost converter and the energy storage voltage regulation. The other section consists of the half bridge, the load, and the controlling of the lamp power. Dividing the path from the mains supply to the load into two nearly independent sections makes system dimensioning very flexible and gives regulation loops that can be optimized individually.

### 3. Controlling the Boost Converter

The input section of the system with the interfaces to the controller of the PFC is shown in Fig. 2. The input signals to the SoC-ASIC are voltages reduced by external resistive voltage dividers. The signals are taken from the mains rectifier output  $V_{RM}$ , the drain connection  $V_{MP}$  of the power transistor  $M_P$  of the boost converter, the shunt  $R_P$ , and the voltage  $V_{bus}$  across the energy storage capacitor. These 4 input signals are fed to the control logic that switches the on-chip driver for the boost converter transistor. The signal processing for the digital boost converter controller is described in detail in [2] and is not in the scope of this paper.

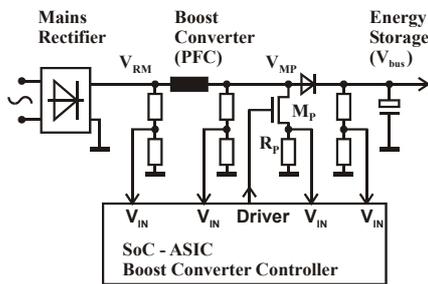


Fig. 2. Input Section of the Electronic Ballast

### 4. Controlling the Lamp Power

The output section of the system with the interfaces to the lamp power regulation is depicted in Fig. 3.

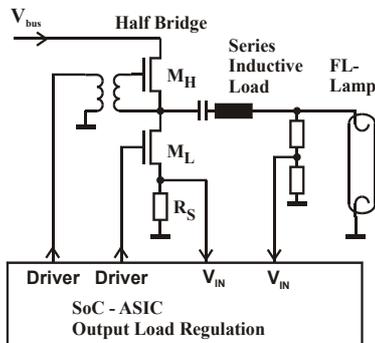


Fig. 3. Output Section of Electronic Ballast

The lamp voltage and the current through the low site driver transistor are taken as the input for the output load regulation, that controls the half bridge drivers. Because of the DC decoupling capacitor the average current through the shunt represents the part of the lamp current that contributes to the real output power. Other measurement principles are possible that measure the current through a shunt at the  $V_{SS}$  connection of the lamp [1]. The low site transistor  $M_L$  is driven directly by

the SoC-ASIC, whereas the high site transistor  $M_H$  is driven by a small transformer performing the level shift from the half bridge output node to ground  $V_{SS}$ . The transformer itself is driven by the common on-chip FET driver.

### 5. Main Blocks of the SOC-ASIC

An overview of the main blocks of our one-chip solution for the electronic ballast is given in Fig. 4. The picture shows the analog interfaces, the support modules and the output drivers. The structure of the digital core section is discussed in part VI of this paper.

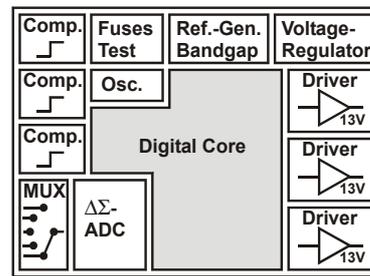


Fig. 4. Main Blocks of the SoC-ASIC

On-chip voltage regulators, bandgap, references, fuses, oscillator and test block contribute to the support functions. The fuses serve for adjustment of voltages, currents and the 10 MHz oscillator, which has an overall accuracy of 3% including initial accuracy and temperature.

Analog inputs are the comparators and the time multiplexed  $\Delta\Sigma$ -ADC. The ADC, together with the decimation filter, gives 12 bit resolution with 3.3 V input range in 100  $\mu$ s. The area of the analog part is 0.25 mm<sup>2</sup> and consumes 700  $\mu$ A, the decimation filter has 5k Gates, including offset and gain calibration running permanently in the background.

Fig. 5 shows the relation between the analog and the digital clock. The comparators and the SC-integrators of the  $\Delta\Sigma$ -ADC are run with the undelayed oscillator clock, whereas the digital core works on a delayed clock from the  $\Delta\Sigma$ -ADC clock generator. This clocking scheme and the intelligent signal evaluation, which skips measurements, while the fast drivers are switching, gives the system excellent noise characteristics.

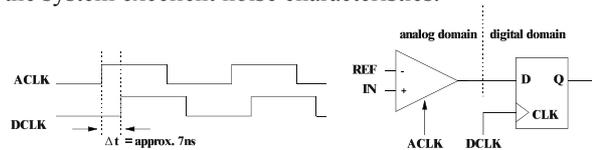


Fig. 5. Clock Interface and Digital Interface

## 6. Digital Design Methodology

Mixed signal design verification is a challenge in the development process. One has to verify the idea, the design and the chip. In the early design phase there is no need to know details about the building blocks. An abstract model is used for the analog part while the digital part is written in a Hardware Description Language (HDL). This way the digital part can be run in an FPGA while the analog part runs in e.g. Matlab/Simulink (see Fig. 6a). This approach is faster than mixed signal simulation.



Fig. 6. Design Verification

As soon as first analog design requirements are established, an analog test chip can be set up to verify the system assumptions (see Fig. 6b). Also the digital part can be developed in detail with a real time test system. The original ASIC HDL code is used although it may be difficult to implement an ASIC design without changes successfully into an FPGA if large arithmetic units are used.

When the characteristics of the analog components are known, they are modelled in HDL to run system level digital simulations (see Fig. 7). This way a common digital design and verification approach can be used to verify the HDL code up to the digital top level. This is used to check the interaction between analog and digital part, especially if digital post layout timing data are available. An FPGA system cannot be used because of the different timing.

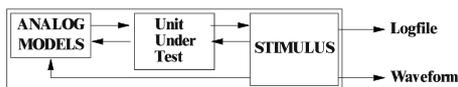


Fig. 7. System Level Verification

The high effort of this methodology is necessary to transfer complex functions from the idea stage to a design (see Fig. 8). A PI regulator is easy to be implemented from a Matlab/Simulink model but a decimation filter could need additional tools like a Signal Processing Workbench (SPW).

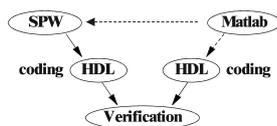


Fig. 8. From Idea to Design

## 7. Digital Functions of the SoC-ASIC

The digital part is split into three functional groups as shown in Fig. 9. These groups are of the categories service blocks to operate the chip, functional blocks to perform the chip's duties and the integration group which connects the digital part to the analog surrounding.

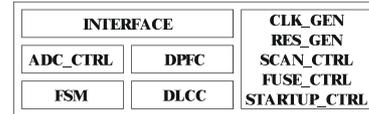


Fig. 9. Structure of the Digital Core

The first group represents the service modules which ensure the basic operation of the chip and consists of the blocks CLK\_GEN, RES\_GEN, SCAN\_CTRL, FUS\_CTRL and STARTUP\_CTRL. CLK\_GEN switches on/off the different clock trees depending on the mode of operation. RES\_GEN distributes the reset signal. SCAN\_CTRL provides all the block connections to the scan test inputs and outputs. It also sets special signals to do some switching in the digital blocks to increase the scan test coverage. The FUSE\_CTRL block contains the fuse programming interface which is also used on the ATE to select the different test modes and analog blocks which are to be tested. It also reads out the fuse values during start-up for reference value adjustments. STARTUP\_CTRL is responsible for a proper startup of the digital system and switches all the different modes of operation e.g. test, scan, fuse and low power depending on the requests given by the logic or the user interface.

The second group consists of the functional blocks. ADC\_CTRL is employed for converting the  $\Delta\Sigma$  bit streams into 12 bit values and sets up the signal select input sequence for the analog multiplexer. The Digital Power Factor Corrector DPFC contains the PI regulator and a distortion improvement block as well as an output signal controller which converts the calculated cycle times into on/off signals for the FET driver [2]. The Digital Lamp Control Circuit DLCC is responsible for calculation of the half bridge output period time and control of the on/off switching of the corresponding FET drivers. Additionally special functions like PWM operation for lamp ignition or immediate shutdown in failure conditions like overvoltage or lamp removal while the lamp is on are implemented in this block.

A finite state machine FSM, as depicted in Fig. 10, contains the control program for all of the system's features. It has a set of eight commands and resources like adders, a timeout counter and an interrupt service block. The FSM is split into the control unit and its ROM part. Thus the system designer is enabled to change the FSM program with minimal impact on the ASIC

designer's work. The ROM table is generated automatically by the customer of one of his flow charts which are checked by system simulation tools like e.g. Simulink. The FSM consists of a 5 bit wide address vector and a 64 bit wide ROM vector.

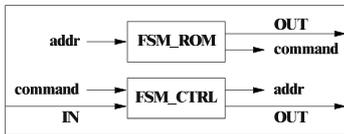


Fig. 10. Finit State Machine (FSM)

The third group contains only one block which controls the interfacing between digital and analog part. It assures that kick back noise from the analog part cannot influence digital inputs. It also provides the switching for test mode control signal and the feedback of outputs if scan test mode is enabled. All signal which cross the analog to digital domain border (and vice versa) are routed through this block, except the global clock and reset signal.

## 8. Measurement Results

The chip foto of the production version of the SoC-ASIC is shown in Fig. 8. A 0.35  $\mu\text{m}$  CMOS process with triple metal, double poly capacitors and high resistive poly yields a total chip area of 4.4  $\text{mm}^2$ .

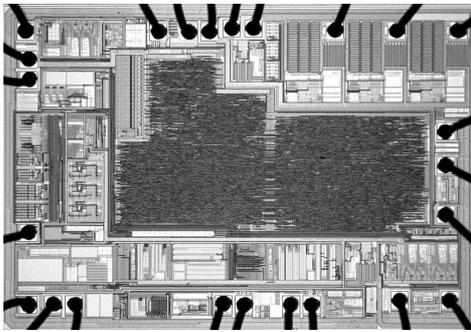


Fig. 11. Chip Photo. Area is 4.4  $\text{mm}^2$

Some measurement results are shown in Fig. 9. Fig. 9a shows the rectified input voltage  $V_{RM}$  (Chan. 1) and the bus voltage  $V_{bus}$  (Chan. 2), both at the ASIC input pins. The upper signal (Chan. 1) of Fig. 9b is the voltage at the drain of the PFC transistor  $V_{MP}$ , the lower signal (Chan. 2) is the driver signal  $V_{MP}$  for the gate of the boost converter transistor.

The upper signals of Fig. 9c and 9d is the rising and falling gate voltage of the low site driver transistor  $M_L$ , the lower signals are the driver signals at the ASIC pin.

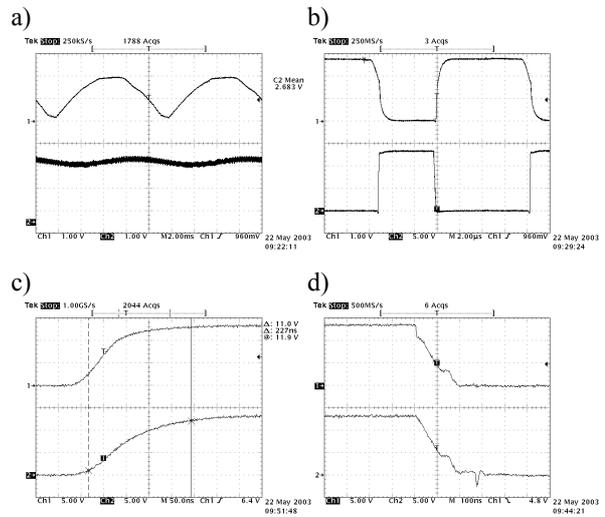


Fig. 12 a) -d). Signals in the 3.3V and 13V Domain

## 9. Conclusions

The one-chip solution presented here is the integration of all control functions of a high integrated smart power electronics system. The integration solution and system topology used for the SoC-ASIC for an electronic ballast can be applied to a variety of power systems for computer and mobile communication system power supplies, for energy saving applications and energy conversion. New packaging technologies [3] becoming popular in future allow easy partitioning of high voltage and low voltage domains and functions which makes our approach with a low voltage IC for SoC integration of power electronics a very attractive solution.

## References

- [1] S. Zudrell-Koch, "Mixed signal ASIC for closed loop fluorescent lamp management using novel digital frequency control strategies", Industry Applications Conference, 2000. Conference Record of the IEEE, Vol. 5, 2000, Pages 3434 – 3440.
- [2] G. Marent, "Novel electronic ballast with integrated digital power factor controller", Industry Applications Conference, 2003. (Accepted paper.)
- [3] Fred C. Lee et. al., "Technology Trends toward a System-in-a-Module in Power Electronics", IEEE Circuits and Systems, Vol. 2, No. 4, 2002.