The perfect HF Receiver. How would it look like today?

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Modern HF Receivers must fulfill a variety of requirements e.g. sensitivity, robustness and many others. Key requirements are often directly leading to RF concepts and architectures with their specific advantages and disadvantages. But how would the perfect HF receiver look like today which combines all available technologies into a most modern concept for a software defined receiver approach?

Is it "IF-Sampling" or "Direct Sampling" or even something else?

First very simple HF receiver concepts have been used 120 years ago and allowed already a transatlantic communication as demonstrated by Marconi. Since then many improvements for the design of an HF receiver have been achieved by introducing new technologies and architectures step by step.
Each technological step was founded on the motivation to achieve specific improvements like smaller size, higher sensitivity or others. In the following the major steps of improvements are summarized:

Step 1: Marconi´s receiver, no amplifiers, no filters but huge antennas.
Motivation for step1: Demonstrate electromagnetic waves as new media for wireless communications.

Step 2: Vacuum tubes for amplifiers and stable oscillators.
Motivation for step 2: Improve range and availability of wireless communication equipment.

Step 3: Improvement of involved components e.g. smaller tubes and better filters.
Motivation for step 3: Reduce size and weight to allow portable equipment during WWII.

Step 4: Introduction of transistors.
Motivation of step 4: Further reduction of **S**ize, **W**eight **a**nd **P**ower (SWaP) and price to allow a mass production.

Step 5: SDR 1st generation introduced
Motivation of step 5: Increase the flexibility by replacing fixed hardwired components by software.

Step 6: SDR 2nd generation.
Motivation of step 6: Further reduce SWaP, tradeoff

This step 7 is now explored in the following.

The architecture of a receiver is directly driven by key requirements which must be fulfilled. The number of key requirements can be quite high but for an HF receiver design there are finally the following three major requirement which are dominating:

*Modern HF receivers must able to pick up **weak wanted signals (1)** while very **strong interferers (2)** are present within a given **frequency offset (3)*** at the same time.

Within these top requirements we have some hidden values which must be known in detail e.g. the required sensitivity, the maximum level for interferers and also frequency offsets between wanted signals and interferers. These three – golden - parameters can and must be extracted from the operational scenario the receiver shall be used in. In combination with the capabilities of typical building blocks e.g. analogue to digital converter (ADC) these three top parameters are determining the best suitable architecture for the receiver. All further parameters within the data sheet of a receiver based on this architecture are now a direct consequence of the quality of the chosen building blocks e.g. phase noise of oscillators as basis for desensitization.

We will start now to assess the three golden parameters and then design the "perfect architecture" being able to fulfill them.

At the beginning we use a general and also very simplified block diagram of a digital receiver to

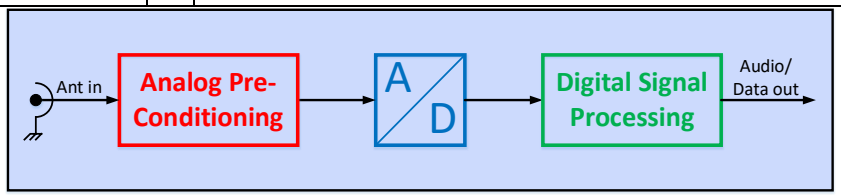
between performance and flexibility.

Step 7: The perfect HF receiver
Motivation of step 7: Best performance with highest flexibility at the same time.

identify how our three golden parameters are influencing the design of major building blocks.

The block diagram of any digital receiver can be built by using three major functional blocks.

- Analogue Preconditioning
- Analogue – to – Digital Converter
- Digital Signal Processing



Δ Fig. 1 General and simplified SDR architecture

In the following the three building blocks are described with some more details:

1. Analog Preconditioning

This block is the coupling element between the antenna input and the input of the ADC. It is setting the correct gain and together with its noise factor it is responsible to achieve the wanted sensitivity of the receiver. It may therefore contain amplifiers and/or attenuators and also elements to adapt the impedance levels if required. Second it may also contain some selectivity to suppress those components of the input spectrum which may be problematic for the ADC. These stages are therefore the main contributors to define the robustness of the receiver.

The selectivity between the antenna input and the ADC may be realized either by inserting filters directly on the operating frequency (pre-selector) or by transferring the input signal to an intermediate frequency (IF filter). Receiver concepts which are not using any intermediate frequency are called "direct sampling receiver" while the use of an intermediate frequency leads to a concept called "IF sampling receiver".

Pre-selector filters on the operating frequency must be tunable or switchable to cover the wanted frequency range of the receiver while IF filters on an intermediate frequency may be operated on a fixed frequency.

The selectivity of pre-selector filters may not be sufficient enough to suppress strong interferers close to the operating frequency of the receiver where weak signals shall be processed. In these cases the designer of the receiver is enforced to choose an IF concept to achieve a required suppression of interferers. The use of an IF frequency allows to include high selectivity filters which will enable the receiver to pick up weak signal very close to strong interferers.

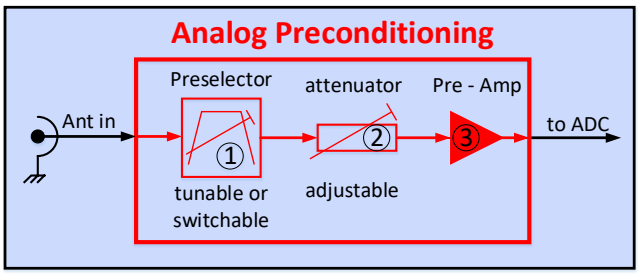
The use of either "direct sampling" or "IF sampling" is therefore only determined by the use case of the receivers. This means that the question "what is the best receiver concept?" cannot be answered without knowing the spectrum requirement at antenna level which has to be fulfilled. In the following we look a bit closer now to the analogue precondition block for

1.1. Analog Preconditioning for direct sampling

Direct sampling concepts require first a carefully designed gain setting between antenna input and ADC. This is done by using an amplifier with a well-chosen gain and noise factor to achieve the required sensitivity of the receiver. Additionally an adjustable attenuator in front of the amplifier allows to shift the operating range of the complete receiver up or down in dependence of the instantaneous spectrum at the antenna.

A pre-selector filter – ideally placed directly at the antenna terminal – provides a minimum required selectivity to protect the ADC but also the preamplifier from strong interferers.

Both parts – gain setting and selectivity – shift the input spectrum at the antenna into an operating window at the ADC input defined by the capabilities of the ADC. The following picture shows these functional blocks:



Δ Fig. 2 Analogue preconditioning for direct sampling

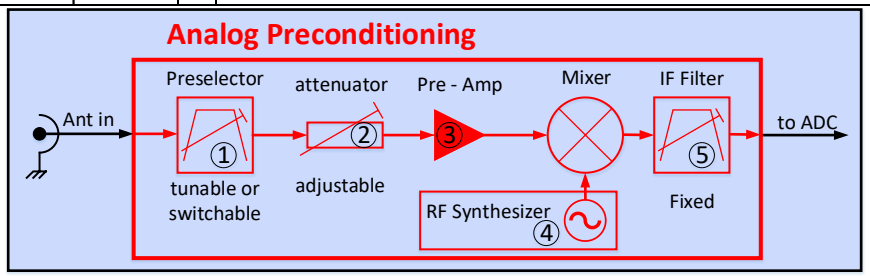
1.2. Analog Preconditioning for IF sampling

IF sampling concepts are transferring the spectrum of the wanted signal to another frequency than present at the antenna. There are two main reasons behind which make an IF sampling concept attractive even knowing that the effort is higher than for a direct sampling concept. One reason is to insert a significantly higher selectivity between the antenna and the ADC and the second is to operate the ADC itself with a higher quality by e.g. selecting the right sampling clock for better performance.

both “direct sampling” and “IF sampling” concepts.

The analogue preconditioning for IF sampling adds two more components compared to the one for direct sampling:

- RF Synthesizer
- IF Filter



Δ Fig. 3 Analogue preconditioning for IF sampling

IF sampling concepts may be the better choice compared to direct sampling in cases where strong interferers are very close to the wanted frequency. In this case the pre-selector filter may not be able to provide a sufficient selectivity to suppress the interferer in a way that the complete spectrum at the input of the ADC is within the operating window of the ADC.

Transferring the input signal to an intermediate frequency allows the use of highly selective filters with shape factors far beyond the quality achievable by a pre-selector at the antenna. But the price to be paid for this advantage of an IF sampling concept is that the mixing process may introduce some significant disadvantages in the spurious performance of the complete receiver. This disadvantage is caused by the fact that the mixing process itself is sensitive to multiple effects e.g. mixing of all harmonics present at the mixer and others. As a consequence the ADC may be operated within an attractive operating window allowing the best dynamic range for this device but the complete receiver may show a rather poor intermodulation performance.

This leads to the situation that the overall performance of an HF receiver concept – either using direct sampling or IF sampling – is always a tradeoff between the individual performances of the used building blocks. In other words an IF sampling concept with a high performance analogue precondition may provide excellent data even when using a poor ADC, or a direct sampling concept using a high performance ADC may not be able to provide good data if the analogue precondition is not defined properly.

2. What is the right concept?

The right concept for an HF software defined receiver is always depending on the use case and the quality of the functional blocks which shall or can be used. The quality of the selected building blocks is then very often influenced by associated costs. As a consequence most of the available HF receivers on the market represent a compromise between available technology and feasible costs, but they normally do not represent what is technically possible if costs were not taken into account.

2.1. What is the perfect concept?

In the following we will try to build up the perfect state – of – the – art concept for a software defined HF receiver by combining the best available technology for each of the required building blocks. We will start our design work with an analysis of available ADCs and the performance they can provide.

2.2. Reading an ADC data sheet

ADC manufacturers are very good in designing their products but they are even perfect in designing their data sheets.

They are promising wonderful data and are proving their promises by using ideal settings. These setting may be based on the best relations between sample rates and the sampled wanted frequencies in combination with well-chosen levels for all involved signals. The given settings within an ADC data sheet may not represent a typical spectrum situation as present for an HF receiver especially with respect to a high level multi signal spectrum.

The designer of a receiver concept must be aware of the relevance of important parameters and how they are influencing each other. Figure 4 shows all major ADC parameters which are important for the design and the quality of a high quality SDR HF receiver design.

At the end it is important how big the difference of levels between weak wanted signals and strong unwanted signals is allowed to be at the input of the ADC. This is finally the most important characteristic being relevant for the design of the complete receiver.

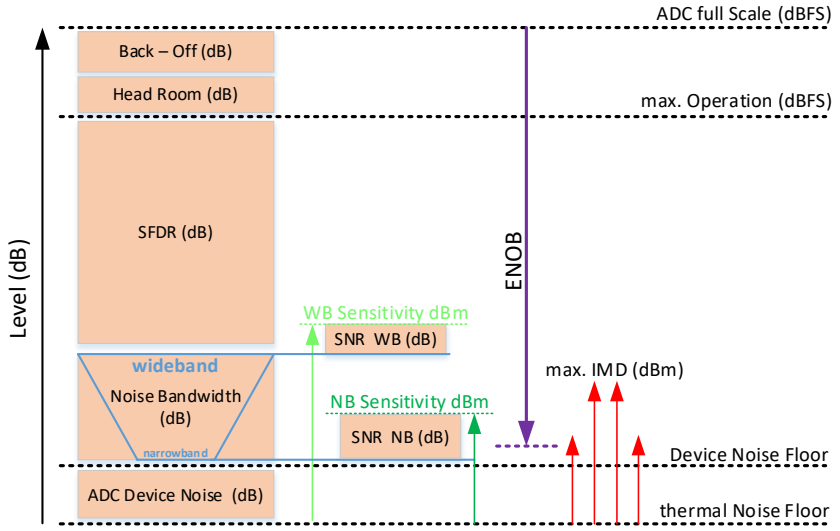
The analysis of an ADC data sheet normally starts with a look to the resolution, noise factor and other parameters which are basically linked to the achievable sensitivity. We will do it here in the opposite direction because it is then easier to understand the behavior of an ADC within the complete architecture of a receiver.

We start with the maximum level allowed at the input of an ADC which is the **ADC Full-Scale-Level**. The amplitude of the sum of signals present at the antenna of the receiver must safely remain below this threshold all the time otherwise the further processing steps are strongly affected and will deliver unusable results.

If strong signals at the antenna are very close to the wanted frequency an automatic gain control (AGC) circuitry has to set the right maximum gain to avoid an overload of the ADC.

The next important parameter is the effective number of bits (**ENOB**). It indicates how far below the ADC Full-Scale-Level a weak signal can be found and identified by the ADC.

It is important to know that a perfect low resolution ADC may have a significant higher ENOB than an un-perfect high resolution ADC.



Δ Fig. 4 ADC parameters at a glance

After sampling the input signals any ADC will show some jitter within the digitized data. Inside this jitter the information of weak signals is hidden and can be extracted e.g. by decimation mechanisms. These decimation algorithms can be seen as a kind of averaging. Averaging across e.g. ten samples may increase the resolution by a factor of ten while also a reduction of the sample rate by the same factor of ten is achieved. This means that decimation algorithms are basically enhancing the effective resolution of the signal processing chain by diving into the noise and jitter at the output of the ADC.

The possible depth of this dive is limited to a point where the jitter of the ADC itself cannot be separated any more from the jitter related to the input spectrum. The jitter from the ADC may also contain jitter from the clock signal therefore it is important that the applied sampling clock is generated with the highest possible quality with respect to phase noise and spurious content.

The value for ENOB does not yet give us any information about the quality of the signal processing chain with respect to intermodulation or any other unwanted signal which has not been present at the input of the ADC but appears at its output.

Unwanted signals at the output of an ADC may be caused by a variety of effects e.g. nonlinearity of ADC input stages or others. These discrete output signals show very often a correlation between the used sample rates and the spectral components of the input signals but are normally not reliably predictable, neither in their frequency nor in their levels. Within a data sheet of an ADC the quality of an ADC with respect to unwanted signals is given as spurious free dynamic range (**SFDR**).The values for SFDR are depending on the settings especially with sample rates, input spectrum and its chosen levels at the ADC input.

It is recommended to evaluate any ADC being a candidate for a receiver design by applying a typical input spectrum including the most likely sample rate to measure the worst case SFDR for this particular use case. This real value may be significantly worse than any promised value taken from the data sheet. This situation makes a direct sampling wideband SDR very critical and highly depending on the quality of the chosen ADC. Any reduction of bandwidth at the input of the ADC is therefore significantly improving the performance of the whole receiver. The price to be paid is now a reduction of the maximum instantaneous bandwidth which can be sampled.

With focus to an SDR receiver especially designed to process the HF band up to 30 MHz while individual signals will always remain narrower than some hundred kHz it can be seen already here that a good pre-selector filter is a must. Any additional "dB" of suppression of unwanted interferer signals will now directly improve the quality of the receiver.

2.3. The best ADC and it´s performance

The ADC is definitely the key component within the concept of a software defined receiver. The dynamic range of an ADC is one of the most important parameters required for the selection of the ADC itself and also of the right receiver concept. For very high RF frequencies (far higher than 30 MHz) the possible operating frequencies might be the only available criteria for the selection of an ADC.

For an HF receiver we need either a direct sampling capability of any frequency up to 30 MHz or the capability to process a fixed intermediate frequency typically below 100 MHz within an IF sampling concept. We will look in the following for the best ADC for direct sampling of signals up to 30MHz being also usable within an IF sampling concept with an IF frequency below but close to 100 MHz.

Several companies are offering ADCs with up to 18Bit resolution using sample rates of up to 100 MHz or even more. The input stages can be operated with bandwidth of some hundred MHz. This would allow to use the same devices with sub-sampling as part of an IF sampling receiver. Sub-sampling concepts are using a sample rate below the sampled frequencies of interest which leads to an effect that the digital output signal is ambiguous which does not clearly allow to identify the original input signal with respect to the frequency domain.

Any sampling concept requires to have a clear knowledge about the input spectrum to be sampled and the used sample rate therefore a sufficient band limitation e.g. with a bandpass filter is required for subsampling. The combination of a bandpass filter with a subsampling ADC would be a valuable backend part of an IF sampling receiver concept.

With modern ADC devices an SFDR of 90 to 100 dB can be expected. This means in simple words that the maximum allowed difference in levels between a weak wanted signal and a strong interferer can be in the order of 90 dB when both signals are applied at the same time at the input of the ADC.

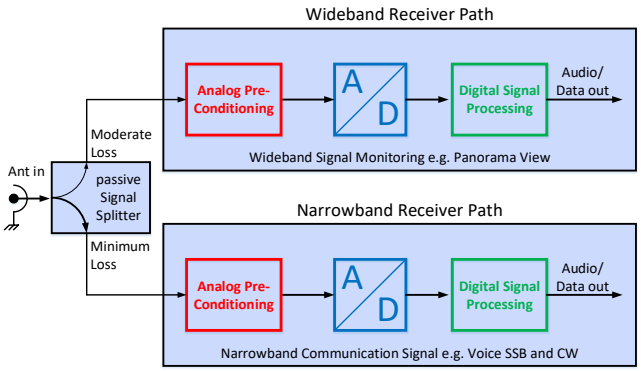
2.4. Starting with the architecture of the receiver

At antenna level especially in the HF band we have to expect a strong multi signal spectrum. Unfortunately the data sheet of an ADC does not tell us anything predictable about the behavior of the ADC when a multi carrier interferer scenario with a high total sum amplitude is applied. As a consequence it is mandatory to reduce the bandwidth of the spectrum at the input of the ADC as much as possible.

2.4.1. Separating Narrowband from Wideband

For use cases where e.g. a wideband panorama spectrum has to be monitored the effective dynamic range may be significant lower than for monitoring a narrowband communication signal. This leads to a situation that the best architecture for receiving wideband signals may or will be different to the one used only for narrowband signals. This does not necessarily mean that two completely different concepts are required. It means at least that the reception of narrowband signals may require completely different settings for HW gains and filters between the antenna and the ADC compared to the ones required for the reception of wideband signals.

The "perfect receiver concept" can adapt to this situation by first splitting the antenna signal into two different paths, one for narrowband signals and for wideband signals, if wideband and narrowband signals must be monitored fully in parallel. The required signal splitter at the input must be designed for a superb intermodulation performance which leads to a passive device. The splitting loss should be chosen unequal and should provide less attenuation to the narrowband path while the wideband path may not be critical influenced by a slightly higher insertion loss. The following picture shows this first step on the way to the perfect receiver concept already.



Δ Fig. 5 SDR Receiver Structure

Both receiver parts may use identical concepts or completely different ones. The minimum difference is at least an individual setting with respect to gain and also pre-filtering between antenna and ADC to adapt best to the different situations with respect to the spectrum to be processed. In the following we will now set up the concept for both receiver paths. The starting point is to analyze the noise situation at the antenna as basis for defining a suitable sensitivity for the receiver.

2.4.2. Limits for Sensitivity → external noise

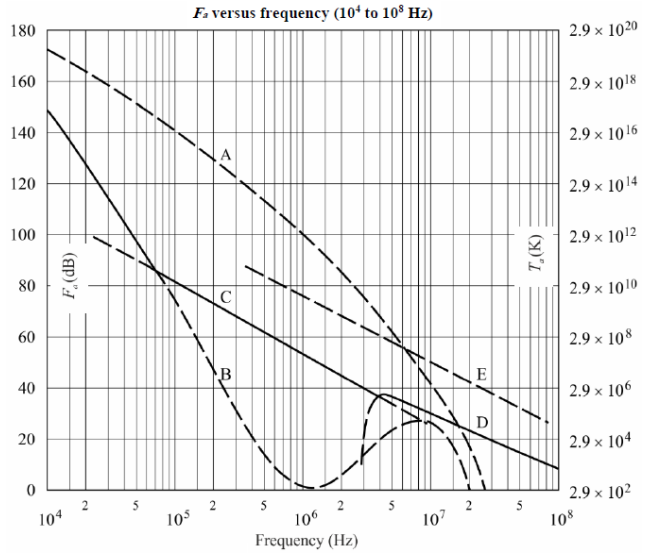
There are two important limits with respect to signal levels at the antenna to be taken into account. One is the maximum level of signals which may occur and the other is the required or possible sensitivity. Both limits are influencing the capability of a receiver to set an appropriate gain between the antenna and the ADC. The possible or required sensitivity is strongly influenced by a noise floor picked up by the antenna and applied to the receiver frontend. This noise floor is variable over time, frequency, location and antenna configuration. As a guideline ITU has created an information which is shown within ITU-R P.272.

Figure 6 gives indications about the external noise picked up by an omnidirectional antenna and then fed to the frontend of the receiver. The different curves (A to E) within graph are representing the following:

A: Atmospheric noise, value exceeded 0.5% of time
B: Atmospheric noise, value exceeded 99.5% of time
C: Man-made noise, quiet receiving site
D: Galactic noise
E: Median city area man-made noise
—— Minimum noise level expected

The intensity of the external noise within the graph is given as equivalent noise figure of a receiver which

allows an easy comparison with the particular noise figure of any given receiver design.



Δ Fig. 6 Noise external to an HF receiver

As a result it is possible to identify those regions where the external noise is dominating and exceeding the noise of the receiver. For these cases it would be basically sufficient to design a receiver with a minimum noise figure being some dBs below the external noise figure.

The expectation related to the capabilities of a modern SDR receiver is to be able to adapt to a variety of situations which might have significant different levels of external noise. The most important factors here are the type of antenna used and especially its geographical location. This means that in silent areas with a minimum of external noise it might be advantageous to have a receiver with a low noise figure while in noisy areas a receiver with a quite high noise figure might be fine to achieve an acceptable system performance with respect to sensitivity.

For silent areas a receiver noise figure of 10dB (or even below) might be perfect while for noisy areas noise figures being tens of dBs higher may be sufficient. The noise figure and therefore the sensitivity of the total receiver is defined by the combination of noise factor, gain and attenuation within the analog pre – conditioning (see Figure 1) between the antenna and the ADC.

2.4.3. Gain, Noise and Dynamic Range

In silent areas a high gain with low noise amplifiers may be used between antenna and ADC while in noisy areas no gain or even an attenuator may be activated. In all cases where no additional hardware filters are inserted between antenna and ADC the dynamic range of the receiver is then equal to or lower than the dynamic range of the ADC. If all elements between antenna and ADC are of high quality the dynamic range of the receiver is equal to the one of the ADC and is just shifted up or down to various absolute levels depending on the selected gain. The maximum usable gain is that one where the strongest signals at ADC still remain below its ADC Full Scale Level. An automatic gain control AGC is used to set the gain continuously to this maximum possible gain. The time constant for the AGC shall be carefully selected to avoid any unwanted gain variations in dependence of either the envelopes of the wanted signals or strong interferers or both. The adaption of AGC time constant parameters to suitable values shall be made either automatically or in some situations even a manual setting may be preferred. The AGC circuitry of an SDR based receiver is different to those known from classical analogue receivers. This is necessary to enable the full dynamic capabilities of an SDR design with respect to bandwidth and also adaptability to a given and probably fast changing spectrum situation at the antenna. The AGC has not only to ensure that the ADC is not overdriven it must also follow the variations of the wanted signal e.g. an SSB voice signal with an appropriate attack and decay time. These requirements may result in an advanced AGC circuitry which separates these two needs and adapts both separately for the best overall characteristic.

2.4.4. Wideband SDR HF Receiver

The main purpose of the wideband receiver path is to monitor a wide instantaneous bandwidth up to the complete HF band. The frequency range may start at 10kHz already or even lower and will go up to 30MHz. It is possible to use a direct sampling SDR concept or transfer the complete HF band to a different frequency level for further processing by using a frequency converter as it is done e.g. within a spectrum analyzer. The frequency conversion will always lead to an IF frequency well above 30 MHz e.g. typically 70 MHz or even higher. In fact it will then require an ADC with a higher performance than for direct sampling because the ADC will be operated on higher frequencies while the expectation for a high dynamic range within a 30MHz bandwidth will not change.

The phase noise and jitter quality of either the local oscillator or the sampling clock is determining the achievable quality for desensitization and selectivity of the total receiver. The requirements with respect to the spectral purity of the local oscillator used for mixing will be higher than those for the sampling clock of a direct sampling concept just based on the different frequency levels. Additionally the wideband mixing concept will have to struggle to achieve a good spurious suppression because there are a variety of effects linked to a wideband mixing concept which may lead to unwanted spurious signals in front of the ADC.

These basic facts and their dependencies are already leading to a direct sampling receiver concept as the best basis for a wideband HF receiver with the capability to monitor up to 30 MHz instantaneous bandwidth. In the following this concept will be completed with additional functional blocks to enable the technically best performance which can be achieved today.

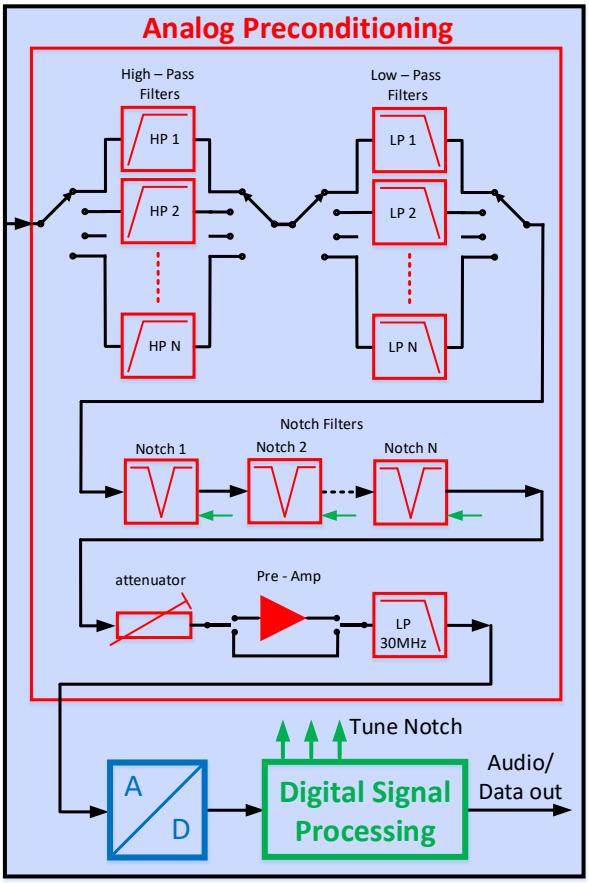
Two key elements within the direct sampling concept are the ADC and the spectral purity of the sampling clock. Further elements between the antenna and the ADC are either optimizing the gain (amplifiers and attenuators) or are limiting the bandwidth (filters). The intention is to place the input spectrum as best as possible into the operating window of the ADC. The assumption is that all elements between antenna and ADC are chosen to provide a sufficiently high quality that they will not be the limit within the design. As an example any amplifier between antenna and ADC must have a very high intermodulation performance beyond the expected performance of the entire receiver. The overall performance of the receiver will then be determined by the setting of gain and filters between the antenna and the ADC.

If filters are selected they are used to suppress strong interferers which will now allow to increase the gain in front of the ADC without exceeding the ADC Full Scale Level. Low –pass and high – pass filters are the best choice if the remaining bandwidth is still high enough for the wanted use case. If the bandwidth shall remain as high as possible at any time notch filters tuned to the strongest interferers are a valuable feature. There are tuning algorithms known which are able to determine the frequency of discrete interferers even in cases when the ADC is already overdriven. Such algorithms can now be used to automatically tune some notch filters to the strongest discrete interferers present at the antenna. In this context it must be mentioned that the used technology for all pre-selector filters shall be selected to provide a sufficiently high intermodulation performance to ensure that they are not the limiting elements of the entire design. Figure 7 shows the completed block diagram of a best performance HF wideband SDR receiver.

The antenna signal first passes pre-selector filters. All elements behind these filters benefit from the existence of these filters already. The filters in Figure 7 are arranged as band-pass configuration built with a combination of high – pass and low – pass filters followed by tunable notch filters. The high – pass filters can additionally act as protective circuits e.g. for electrostatic discharge or lightning protection to a certain amount.

The combination of high – pass and low – pass filters provides the advantage to vary the passband.

bandwidth while keeping a high selectivity at the edges of the filters which gives a high flexibility to adapt to the spectrum situation at the antenna. The notch filters are cascaded and can be tuned fully independent from each other.



Δ Fig. 7 Wideband HF receiver

All filters may use switched inductors and/or switched capacitors to achieve a sufficient tuning range while providing excellent intermodulation performance.

Behind the filters a settable attenuator follows which is in front of a high linearity pre-amplifier. The amplifier can additionally be bypassed. The attenuator plus the amplifier bypass capability are used to set the gain of the entire signal path between the antenna and the ADC.

The filter and amplifier section is building the analog preconditioning section as shown in figure 2 already. Behind the high end ADC the digital processing section follows. This section is likely to be built using FPGA circuits for proving the sampling signal plus configurable building blocks for digital signal processing. The digital signal processing will start with some initial digital filters and digital downconversion. After the digital downconversion the sample rate is normally low enough to allow a further processing within DSP chips.

The current trend for digital signal processing is to avoid dedicated DSP chips and place all signal

processing stages within FPGAs only. The advantage of operating all signal processing blocks inside an FPGA is that many blocks can be operated fully in parallel. This allows to run processing blocks which are responsible for tuning the notch filters, setting the. optimum gain and others related to preconditioning completely separated from those blocks which are linked to the used waveforms e.g. demodulators and audio filters. With this configuration it is possible to set the required gain very fast while the demodulation process has not even started which enables the receiver to adapt to any spectrum situation at the antenna with a very high speed.

The capability of operating many signal processing blocks fully in parallel is perfectly matching to a direct sampling SDR design because it also allows to run many different user applications in parallel

This opens up the way to a very convenient and comfortable receiver as a product providing e.g. panorama views, spectrum monitoring, demodulation of various signals and others fully in parallel at the same time. The only constraint is that all applications are operated within the same gain and filter settings and operating window of the ADC. Nevertheless due to the capability to set e.g. gain very fast it is basically possible to assign different gains and filter settings within a time sharing concept to different applications as long as the reserved time slots are sufficient for them.

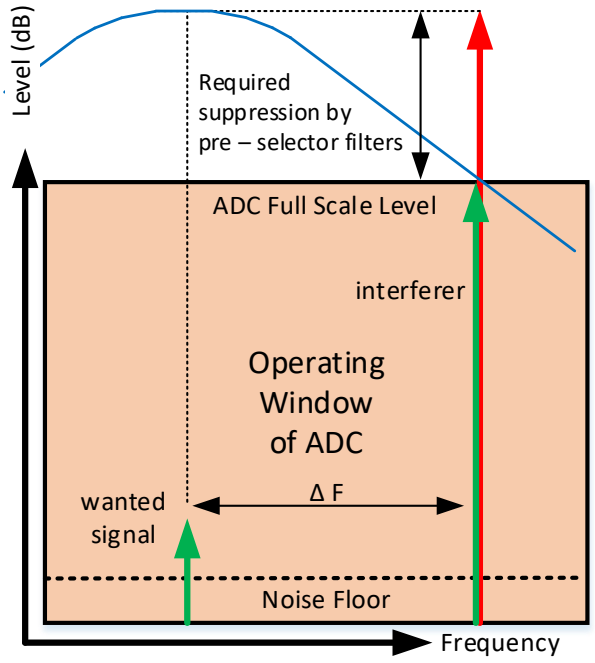
2.4.5. Narrowband SDR HF Receiver

The concept behind the wideband receiver design was mainly driven by one single key requirement which is the ability to operate an instantaneous bandwidth of up to the entire HF band. The signal processing stages are not limited to process either wideband or narrowband signals. This leads to the question why a narrowband receiver might have a different concept. The answer to this question is directly linked to the use case or in other words: Where is the receiver operated and what is the situation with respect to noise, interference and frequency offsets between interferers and wanted signals?

In some use cases strong interferers may come very close to the frequency of the wanted signals. The AGC will now reduce the gain between antenna and ADC to a value which ensures that the ADC is not overdriven. But if the difference in levels between the wanted signal and the interferer is higher than the dynamic range of the ADC the total receiver will now not be able any more to find the wanted signal because it is shifted below the sensitivity threshold of the receiver.

The way out of this situation is to suppress the interferer by using filters between antenna and ADC. The required selectivity and suppression of the filter for this use case is this value in dB by which the difference of levels between wanted signal and interferer is exceeding the dynamic range of the ADC. As an example if the dynamic range of the ADC is equal to 100dB and the interferer is 120 dB above the wanted signal then we will need at least 20 dB suppression of the interferer by the pre-selector filters. Figure 8 shows this situation.

The wanted signal (small arrow in green) is close to the sensitivity of the system at the input of the ADC and the strong interferer in red is some dBs above the ADC Full Scale Level. The blue curve shows the selectivity of the pre - selector filters in total. The suppression of the pre – selector in a frequency offset of ΔF is sufficient in this example to reduce the level of the interferer below the ADC Full Scale Level. The reduced interferer signal (the long arrow in green) and the wanted signal (small arrow in green) are now both within the operation window of the ADC. The frequency offset ΔF is the frequency difference between the wanted signal and the closest interferer which may be beyond the ADC Full Scale



Δ Fig. 8 ADC Operating Window with Pre - Selector

These easy facts are now giving a clear advice which concept to be used or is best for an SDR HF receiver.

- If the selectivity of the pre-selector filters is good enough to bring any spectrum situation into the operational window of the ADC and the wanted sensitivity is still available then a direct sampling concept is usable and is recommended.
- If the selectivity of the pre-selector filters is not sufficient then an IF sampling concept is a must because the missing sensitivity can only be added within the IF domain.

These two statements are expressing that the choice between a direct sampling concept and an IF sampling concept is only based on the required selectivity between the antenna and the ADC in combination with the capability of the ADC. The flexibility of a direct sampling concept is higher than for an IF sampling concept because the digital signal processing has a wider access to the spectrum. Therefore it is recommended to start first with a direct sampling approach and then try to extend its performance to the technological maximum or to the technological need based on the use cases by selecting a suitable high end ADC and high performance pre – selector filters.

In cases where the dynamic range in combination with the pre – selector´s capability is still not yet sufficient an IF sampling approach should then be selected. If an IF sampling concept is the only way to fulfill the wanted spectrum requirement it can to be taken into account that the insertion of an IF filter as such will already introduce a quite high additional selectivity compared to the pre – selector. This means that after selecting an IF sampling concept an optimization is possible by either relaxing the ADC performance requirements or those of the pre – selector filters or both. These steps will help to reduce costs by enabling the use of cheaper key components for the design.

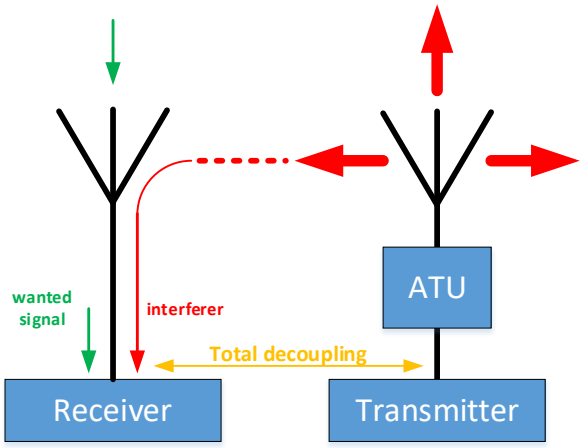
In the following costs will not be taken into account and further thoughts about concepts are only driven by trying to maximize the performance to a limit defined by the available technology for key components.

2.4.5.1. Define the Data sheet for a high end Narrowband SDR HF Receiver

We assume that the planned receiver shall able to provide a high sensitivity (if required) while strong interferes may be present at the same time. Interferers are allowed to come as close as e.g. 10% from the tuned center frequency of the receiver which is the case within some collocated installations e.g. Navy Ships or Costal Stations. Interferers in such a small frequency offset may introduce some external noise to the receiver caused by the transmitter sideband noise. This means that a receiver must be able to operate with the high level of interferer being present at the antenna but at the same time the required sensitivity can be adapted to the external noise caused by the transmitter. This means that the creator of the data sheet for a high end receiver must know or at least assume the characteristics of the interferer signals and their installation close to the receiver.

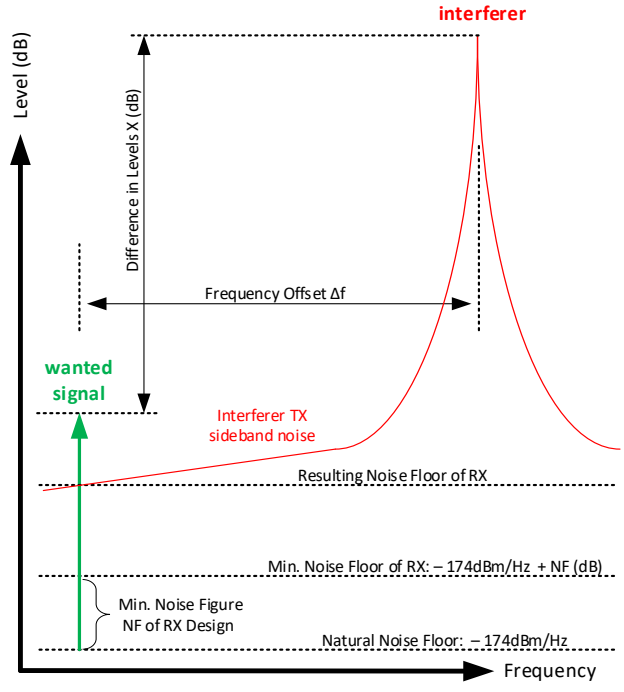
Figure 9 shows that very strong interferes are normally part of the same system installation where the receiver is part of. Ideally the designer of the receiver is also the system designer of the installation including the.

installed transmitters. This means that the design work should ideally focus on a transceiver concept where the receiver is a part of it including the selection and placement of all relevant antennas.



Δ Fig. 9 Collocation Scenario for the receiver

The worst case situation for the receiver is given when a very low noise transmitter is acting as interferer and the system is operated in a quiet area. For a quiet area we assume a noise figure of 10 dB should be achievable by the receiver. The required tolerable difference in levels between wanted signals and interferers can be estimated by analyzing key parameters within the system installation. The next picture shows these key parameters and in the following real values are given as basis for further calculations.



Δ Fig. 10 Key Parameters for collocated Installations

For the key parameters within figure 10 the following values are assumed:

- Frequency Offset ΔF: 10%
- Total decoupling: 15 dB
- Excellent Interferer TX Sideband Noise: 180 dBc/Hz @ 10%
- Interferer Transmit Power: 1000 W

The value for the total decoupling between TX output and RX input is based on typical parameters for all relevant parts e.g. ATU efficiency, antenna types and distances between antennas within big communication sites. It is known that even smaller values for decoupling may be present but these are seen as an exception.

The data for the sideband noise of the interferer are beyond those of currently fielded transmitters. The reason is that it is assumed that not only SDR receivers but also SDR transmitters will improve over the next years. With these primary information some important data at the receiver input can be derived. The estimation of levels for wanted signal requires to use some further assumptions for the used waveform related to bandwidth and SNR. We choose here either A1A (CW) with a bandwidth of 200 Hz or an SSB signal J3E with a bandwidth of 3000 Hz. For both we assume an SNR of 6 dB knowing that A1A signals can be reliably picked up with significant lower SNR. The reason for using the same SNR is to show the influence of the used bandwidth only which allows an easier comparison of parameters.

- Level of Interferer at RX input +45 dBm
- Noise Power Density of Interferer at RX Input: -135 dBm/Hz
- Equivalent Noise Figure of RX with Interferer: 39 dB
- Noise figure of RX without Interferer: 10 dB
- Usable Levels for wanted Signals without Interferer:
    - A1A: -135 dBm or 0,04 µV
    - J3E: -123,2 dBm or 0,15 µV
- Required Levels for wanted Signals with Interferer:
    - A1A: -106 dBm or 1,1 µV
    - J3E: -94,2 dBm or 4,4 µV
- Difference in Levels between Interferer and wanted Signal:
    - A1A: 151 dB
    - J3E: 139,2 dB

The challenge for the planned receiver concept is now to tolerate a very strong interferer of +45 dBm at a frequency offset of 10% while a wanted SSB signal which is 139 dB lower has to be demodulated properly. For the reception of A1A the weak wanted signal is even 151 dB lower than the interferer at the antenna. In cases where an A1A signal shall be picked up this difference in levels increases accordingly if the SNR shall be less than 6 dB as chosen here.

If we assume that in practice a high end ADC is able to operate weak signals 100 dB below the ADC Full Scale Level we can assume that with some SNR required the maximum allowed difference in levels between an interferer and a weak wanted is 95 dB maximum. This value will be available if the AGC of the receiver is able to set the gain between antenna and ADC very precisely and carefully and is now taken as basis for further calculations.

2.4.5.2. Thoughts about Pre – Selector Filters

We know now that the pre - selector must provide the missing suppression of the interferer beyond the 95 dB ADC range which leads to a required selectivity of 56 dB @ 10% offset if the receiver shall be able to pick up narrowband A1A signals. If it is sufficient to operate only J3E signals the required selectivity will be approximately 44 dB @ 10%. These values required for the pre - selector filters are pointing to a well-defined high end design of all elements between antenna and ADC not only the filter stages as such. The input level of +45dBm must not lead to any relevant nonlinearity which is already very difficult to be achieved independent from the basic SDR concept for the rest of the receiver.

The pre – selector must provide an electronically tunable band – pass characteristic through almost the whole HF – band from 1,5 MHz up to 30 MHz. Below 1,5 MHz it is seen as sufficient to use a 1,5 MHz low – pass filter because in this part of the HF-band the interferer scenario is significantly different to the one above 1,5 MHz.

A reasonable limit for an achievable value for selectivity in combination with a sufficiently low insertion loss and a very high power handling capability is seen to be at typical 20dB suppression @ 10% offset for one filter stage. This value for selectivity must also be seen in combination with temperature stability and finally the size of the required components like inductors and capacitors plus elements for switching e.g. relays. If the absolute power was lower a more selective design would be possible but as shown before selectivity is not the only important parameter to be fulfilled.

The pre – selector will consist of several filters which are dividing first the entire band into sub-bands. This allows to keep the individual complexity of a particular filter within some practical limits. The required total selectivity can then be achieved by cascading filter stages by using amplifiers in between. These amplifiers must also be of a high linear design and will be combined with attenuators and a switchable bypass to allow a proper adaption to different input spectrum situations.

The quality of the components between antenna and ADC, we called it Analog Preconditioning already, is essential for the overall performance of the total receiver. Independent on whether the receiver concept is finally a direct sampling or an IF sampling concept the Analog Preconditioning stages are just responsible to reduce unwanted interferers sufficiently enough to allow a linear operation of all following components.

Protecting the mixer within an IF sampling concept is of the same relevance as protecting the ADC within a direct sampling concept. The essential difference between IF sampling and direct sampling is just the following: An IF sampling concept can dive deeper into the noise parts of the spectrum after the pre selector filters than a direct sampling concept can do. The reason is just because the IF filters are providing an additional selectivity in front of the ADC suppressing strong interferers beyond the capabilities of the pre – selector filters. This means that if a "super performing pre – selector" was possible a direct sampling concept would be the best choice because it avoids some unwanted additional spurious which may be created by the mixing process. For real pre – selectors even high performing ones an IF sampling concept is a must beyond a particular limit for strong interferers.

2.4.5.3. Block Diagram of an High End SDR HF Receiver

If the data sheet as shown within section 2.4.5.1 has to be fulfilled then an IF sampling concept is the best choice. In figure 11 a block diagram for such a high end SDR receiver is shown. After the block diagram the receiver data sheet is shown in detail.

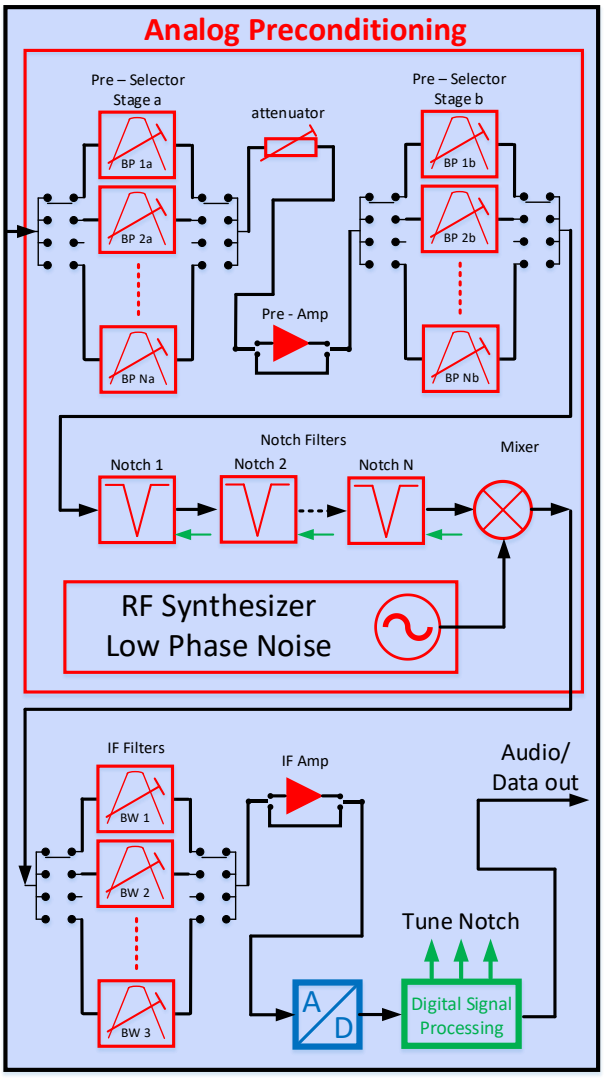
The block diagram shows all required key elements to build a high end SDR HF receiver with the capability to operate very narrowband signals e.g. A1A with 200Hz bandwidth even in the presence of strong interferers.

The antenna signal first passes a two stage pre - selector built with tunable band- pass filters. The band – pass filters are covering the HF-band from 1,5 MHz up to 30 MHz. The frequency range below 1,5MHz can be operated by using a 1,5 MHz low – pass filter instead of the band – pass filters which is not shown within the block diagram.

The pre – selector uses two cascaded filter stages with a combination of attenuators and amplifiers in between. With deactivated attenuator and activated amplifier a total noise figure of 13 dB can be expected. This value is some dBs more than the 10 dB used as design goal within the previous chapters but still provides a very good sensitivity for quiet areas

If we take into account that the narrowband receiver is combined with a wideband receiver within the same box and the signal from the antenna is split (unsymmetrical) to the two receiver paths we can calculate with a total noise figure of typical 15 dB.

Using a much easier symmetric split (e.g. with 3 dB coupler) will lead to at least 16dB noise figure or even higher. Nevertheless an unsymmetrical split is possible by using the right circuits and impedances so we will proceed with 15 dB noise figure.



Δ Fig. 11 High End SDR Receiver Block Diagram

The selectivity of the pre – selector is expected to be at least 40 dB @ 10% offset. With the additional notch filters behind the band - pass filters some discrete interferers can be further reduced. This leads to an assumption that with such a pre – selector an interferer suppression at an offset of 10% or more can be taken to be at least 60 dB.

When using an IF sampling concept we should be aware that all analog stages like the mixer will show the "classical" intermodulation behavior expressible by e.g. IP3. Due to the fact the ADC is not offered a wideband spectrum any more it can be expected that the complete receiver will show an intermodulation behavior similar or identical to a classical analog receiver.

After passing the pre – selector the signal is fed to a high level mixer. At this point an interferer with the maximum allowed level of +45 dBm @ 10% at the antenna will still be as high as -10 dBm at the mixer input if we assume the total selectivity of the pre – selector is 60 dB. This value is achieved by a combination of the 40 dB selectivity of the band – pass filters plus an assumed suppression of some additional 20 dB by the notches. Notches may be able to easier provide a sufficient additional suppression of strong single interferes compared to other type of filters therefore a combination of notches together with other type of filters may lead to a simpler pre-selector design in total.

We have to ensure that this high level of the interferer must not cause any saturation of the mixer nor a desensitization based on the phase noise of the local oscillator. Effects caused by reciprocal mixing are leading to a reduction of sensitivity in the same way as the phase noise of the interferer is already doing. The goal for choosing the right phase noise quality for the local oscillator should be that desensitization effects of the receiver should be some dBs less (ideally 10 dB) than the effects from the interferer phase noise. This will ensure that only the quality of the external signal is limiting the overall performance and not the receiver. In chapter 2.4.5.1 we assumed the phase noise of the interferer to be as low as -180 dBc/Hz @ 10% offset. After the pre- selectors the carrier of the interferer is reduced by the selectivity but not the noise which falling directly into the receive channel. This means that the effective required phase noise quality for the local oscillator can be relaxed by the same amount of dBs as the pre – selector provides suppression of the interferer´s carrier level.

Figure 12 shows this positive effect. The red curve within the picture shows the interferer with its sideband noise. The carrier noise at a frequency offset of 10% is directly falling into the receive channel and will be directly converted into the IF filter behind the mixer. The picture is placing the green IF filter at a position within the spectrum which is equal to the receive channel at the antenna because all signals here will transferred into the IF filter after the mixer. After the pre – selector the level of the red carrier is suppressed while the noise falling into the receive channel is unchanged. We are summarizing these values in the following:

- Relative Phase Noise of Interferer at Antenna:

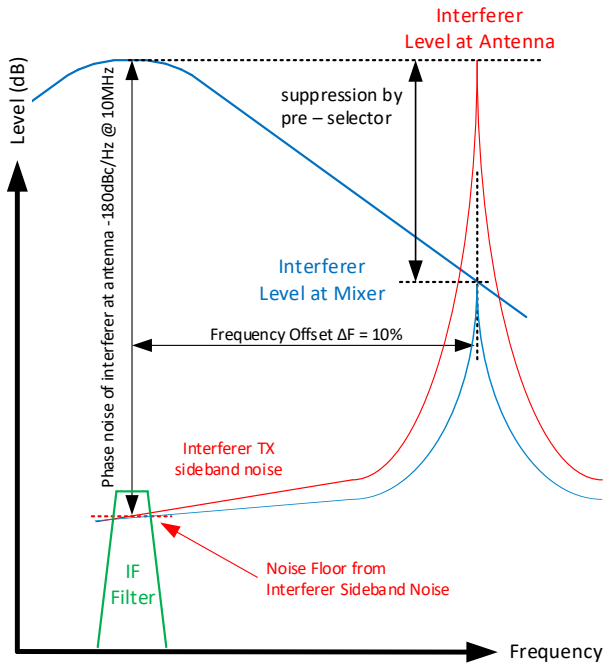
  -180 dBc/Hz @ 10%

- Total Attenuation of Pre – Selector between Antenna and Mixer:

  60 dB

- Relative Phase Noise of Interferer at Mixer Input:

  -120 dBc/Hz @ 10%



Δ Fig. 12 Phase Noise at Mixer

This simple calculation shows how important the selectivity of the pre – selector is for the overall performance of the receiver. Any improvement of the selectivity by e.g. X dB reduces the requirement for all components behind by the same amount of X dB. The local oscillator within an IF sampling concept has exactly the same relevance as the sampling clock of a direct sampling concept. The lower the quality of the pre – selector the higher the requirements for LO phase noise or sample clock phase noise plus quality of the ADC. A local oscillator with poor phase noise will cause a reduction of sensitivity of the receiver in the presence of interferers even if these interferers have an excellent low carrier noise.

For the local oscillator our receiver we can assume that we need at least a phase noise of -130 dBc/Hz at the same absolute offset as the interferer has at the antenna. The IF frequency is expected to be at typical 70 MHz. It is recommended to foresee a slight variation of this IF frequency to avoid some negative constellations between input frequency, LO frequency and IF frequency which may lead to some spurious signals within the IF. Within our block diagram of the receiver shown in figure 11 some switchable IF filters are shown which allow not only to change the IF frequency but also select different bandwidth values.

The tuning range of the LO will be typical 70 MHz to 100 MHz. The worst case situation for the LO phase noise is given when the receiver is tuned to 1,5 MHz where the -130 dBc/Hz phase noise requirement must be fulfilled at an offset of 150 kHz which is 10% of 1,5 MHz. It is recommended to carefully design the LO Synthesizer for lowest phase noise and lowest

spurious because this is another key element being responsible for an excellent performance. With a low noise VCO at typical 1 GHz followed by a divider a. phase noise of beyond -150 dBc/Hz can be expected for the required LO frequencies. The fine tuning of the LO can be done using a hybrid synthesizer using a combination of a direct digital synthesizer DDS with a PLL based cleaning loop.

A level of +17 dBm for the LO signal at the mixer is seen to be sufficient with the chosen pre – selector performance. But it must be recognized that with a reduced quality of the pre- selector the LO level must go up because the interferer level will go up as well. In parallel the phase noise quality must also go up. If an LO synthesizer with a phase noise of -150 dBc/Hz is taken then theoretically the selectivity of the pre – selector can be released from the current 60 dB to 40dB. This will then lead to an increase of the interferer level after the pre – selector of +5 dBm which is very high even for high level mixers with +27 dBm LO level. As we are trying to setup the perfect concept for an SDR HF receiver we therefore should chose a very low noise synthesizer for the LO signal AND the high selectivity of the pre – selector at the same time

2.4.5.4. The final data sheet and the specification of key components

Based on the block diagram shown within figure 11 the SDR HF receiver is basically able to fulfil a data sheet which is shown in the following. This data sheet strongly depends on the quality of some key components which are also stated.

The data sheet of the receiver was derived from the following cosite scenario with reference to figure 9:

For military installations:

- Frequency Offset ΔF: 10%
- Total decoupling: 15 dB
- Interferer Transmit Power: 1000 W

For amateur radio installations e.g. field days:

- Frequency Offset ΔF1 within same amateur band: 100 kHz
- Frequency Offset ΔF2 to the next amateur band: >10%
- Total decoupling: 25 dB
- Interferer Transmit Power: 150 W

We must be aware that a high end receiver will not be able to show its full performance in the presence of low end transmitters. This fact mandates that we also have feasible value for transmitter sideband noise available for both scenarios. The parameters stated in the following are beyond those of currently fielded transmitters because we assume a step ahead in the capabilities for the transmitter within the next years as well.

- Excellent Interferer TX Sideband Noise: -150 dBc/Hz @ 100 kHz
- Excellent Interferer TX Sideband Noise: -180 dBc/Hz @ 10%

The sideband noise at an offset of 100 kHz is determined by the synthesizer concept within the transmitter while the value at 10% can be achieved by using additional so called cosite filters at the right position within the block diagram. These cosite filters can be switched into the receive chain and then reused as pre -selector filters in receive mode.

Data sheet of the high end SDR receiver:

- Tuning range: 10 kHz up to 30 MHz
- Max. Noise figure of RX without Interferer with Pre – Amp on:
  - Path 1 Wideband: 10 dB
  - Path 2 Narrowband 15 dB
- Max. allowed Difference between Interferer and wanted Signal:
  - Path 1 Wideband:
    - A1A (200Hz): 95 dB
    - J3E (3000Hz): 95 dB
  - Path 2 Narrowband:
    - A1A (200Hz): 150 dB
    - J3E (3000Hz): 140 dB
- Sensitivity of RX without Interferer (pre Amp on)
  - Path 1 Wideband:
    - A1A (200 Hz): -135 dBm or 0,04 µV
    - J3E (3000 Hz): -123 dBm or 0,16 µV
  - Path 2 Narrowband:
    - A1A (200 Hz): -130 dBm or 0,07 µV
    - J3E (3000 Hz): -118 dBm or 0,28 µV
- Sensitivity of RX with Interferer present
  - Use case 1 military: 1000 W with -180 dBc/Hz @ 10% and an antenna decoupling of 15 dB
  - Use case 2 amateur: 150 W with -180 dBc/Hz @ 10% and an antenna decoupling of 25 dB
  - Use case 3 amateur: 150 W with -150 dBc/Hz @ 100 kHz and an antenna decoupling of 25 dB
  - Path 1
    - Use case 1 (with pre - selector >55 dB@10%):
      - A1A (200 Hz): -106 dBm or 1,12 µV
      - J3E (3000 Hz): -94 dBm or 4,46 µV
    - Use case 1 (without pre - selector):
      - Any mode - 50 dBm or 710 µV
    - Use case 2 (with pre - selector >55 dB@10%):
      - A1A (200 Hz): -124 dBm or 0,14 µV
      - J3E (3000 Hz): -112 dBm or 0,56 µV
    - Use case 2 and 3(without pre - selector):
      - Any mode - 68 dBm or 89 µV
  - Path 2 Narrowband:
    - Use case 1:
      - A1A (200 Hz): -106 dBm or 1,12 µV
      - J3E (3000 Hz): -94 dBm or 4,46 µV

- Use case 2:
  - A1A (200 Hz): -123 dBm or 0,16 µV
  - J3E (3000 Hz): -111 dBm or 0,63 µV
- Use case 3:
  - A1A (200 Hz): --94 dBm or 4,46 µV
  - J3E (3000 Hz): -82 dBm or 18 µV

Specification of key components within the block diagram:

- ADC
  - Path 1: 16 – 18Bit, >100MSPS
  - Path 2: 14 - 16Bit, subsampling
- Pre – Selector filter stages (band - pass)
  - Path 1: a set of fixed high – pass and low – pass filters, selected via RF Relays, insertion loss 2dB per Filter
  - Path 2: a set of band – pass filters, tuning by switching inductors and capacitors via RF Relays, insertion loss 4dB, selectivity 20dB @ 10%
- Pre – Selector filter stages (notches)
  - Path 1: a set of tunable notch filters, tuning by switching inductors and capacitors via RF Relays, insertion loss 2dB, suppression 20dB @ 10%
  - Path 2: a set of tunable notch filters, tuning by switching inductors and capacitors via RF Relays, insertion loss 2dB, suppression 20dB @ 10%
- Pre – Amp between the pre - selectors
  - Path 1: gain 15 dB, noise factor 5 dB, P1 dB > 10 dBm
  - Path 2: gain 15 dB, noise factor 5 dB, P1 dB > 40 dBm
- Switchable attenuator range
  - Path 1: up to 60 dB
  - Path 2: up to 30 dB
- Mixer
  - Path 1: not applicable
  - Path 2: high linearity double balanced passive mixer, LO level +17 dBm → +27 dBm
- Quality of sampling Clock or local Oscillator
  - Path 1: -140 dBc/Hz @ 150 kHz (→ 150 dBc/Hz)
  - Path 2: -140 dBc/Hz @ 150 kHz (→ 150 dBc/Hz)
- IF filters before ADC
  - Path 1: not applicable

Path 2: two sets of band – pass filters at 70 MHz and 70 MHz + x, various bandwidths between 250 KHz and 500 Hz with t.b.d. values in between. Current wideband HF data communication waveforms are defined for bandwidths of up to 240kHz. Future versions may use even more bandwidth e.g. up to 1MHz. Therefore it may be feasible to preplan IF filters with a suitable higher bandwidth already.

3. Conclusion

Both direct sampling and IF sampling are state of the art concepts for high end SDR HF receivers. For wideband receivers direct sampling is the clear choice while for narrowband receivers an IF sampling concept is recommended. For a high end receiver providing e.g. a panoramic view of the entire HF band while narrowband signals are operated in parallel it is recommended to use two separate and independent receiver paths representing the two SDR receiver concepts.

The capability of an IF sampling receiver is highly depending on the quality and performance of the pre-selector between antenna and ADC. With some well chosen combinations of high – pass and low-pass filters plus some notches (composite filters) a highly performant and flexible pre – selector can be built which shifts the total capability of an IF sampling receiver to excellent parameters. As a rule of thumb an IF sampling receiver with a good pre – selector is well usable if other stations are separated by typical 40 dB antenna decoupling. With lower antenna decoupling values some additional selectivity is required which can only be added on an intermediate frequency.

4. Outlook

4.1. SDR HF Receivers

Beyond the basic SDR concept of a high end HF receiver some optional enhancements can provide more operational benefits for the user. Direct sampling receivers can be realized quite compact which allows now to couple e.g. two separate signal paths to build a diversity configuration. With two different antennas including e.g. optional different polarization some interesting capabilities like fading compensation, interferer nulling and others can basically be achieved. These new applications are still at the beginning but with cheaper and smaller but high performing direct sampling SDR HF receivers these new capabilities will be state of the art in some years.

4.2. SDR HF Transmitters

High end SDR HF receivers can be designed to tolerate high level interferers while the receiver is still able to provide a high performance. The overall performance of a receiver in the presence of strong interferers is influenced by the quality of these interferers. Therefore it is important that also the design of modern transmitters are improving to allow a total improvement of the capability of installations where receivers and transmitters are collocated to each other.

Modern SDR HF transmitters can achieve excellent performance with respect to phase noise if the signal generation is using full digital mechanisms followed by a well defined chain of amplifiers and filters. The nearby phase noise e.g. at an offset of 100kHz is

exclusively determined by those circuits which are generating the carrier signals. In many fielded systems a low phase noise analogue oscillator stabilized by a high quality phase locked loop is the preferred solution. In future transmitters a full digital solution will provide the transmit signals with a better phase noise which are also already modulated. The use of these digital circuitries will allow to simplify the block diagram by getting rid of analogue mixers and modulators.

Nevertheless transmitters using analogue oscillators are still able to provide excellent data with respect to phase noise if the details within their design are well chosen. Figure 13 shows the measured phase noise for a high end transmitter achieving -150 dBc/Hz @ 100kHz offset with a carrier frequency at 14.2MHz.

Δ Fig. 13 Phase noise of an analogue Transmitter

These values have been the basis for one of the chosen three cosite scenarios before within this article. The tested transmitter achieves a phase noise of better than -160dBc/Hz @ 300kHz and with some optional filter modules even significantly better values are available

Beyond the advantages of a better phase noise performance in combination with a reduced complexity of the block diagram digital solutions for transmitters are also enabling more features like an active linearization or some advanced power regulation mechanisms which are working stable even in the presence of strong backward interferers.

4.3. SDR HF Transceivers

Almost all SDR HF receivers and transmitters are part of the same transceiver unit. This allows to reuse core building blocks for both receiver and transmitter part. These core building blocks are mainly frequency generation and filter functions. The low noise signal generation can provide not only the transmit signal but also the low noise Local Oscillator for an IF sampling receiver.

In the same way the receivers pre - selector filters can be switched into the transmit signal chain during transmit operation and will reduce any out of band emission e.g. noise and also discrete spurious.
A low transmitter noise floor (lower than the used -180dBc/Hz within this article) will be achieved if the pre – selector appears within the transmit chain at levels of at least +20dBm. This level corresponds to those for strong interferers in receive mode.
The technical data for some building blocks can and should be harmonized between the data sheet of transmit mode and receive mode. This is given if a cosite scenario is used where two identical transceivers are used as receiver and as interferer. The phase noise at low frequency offsets will define the quality of the interferer transmitter noise but also for the receiver with respect to reciprocal mixing if both paths are using the same frequency synthesizer. The same situation is given for the pre – selector which shall be inserted at a power level within the transmit chain which is similar to the level of the strongest interferer in receive mode.
With this strategy the main data for receiver and transmitter parameters can be derived which leads to the best possible system performance e.g. sensitivity at a given antenna decoupling and frequency offset can be achieved.

This article can be found in a compact version within the printed version of the MWJOURNAL

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